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Hardware-Efficient CNN Design Using Approximate Multipliers and Adders for MNIST Classification

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Abstract

The increasing demand for energy-efficient deep learning systems has driven significant research in hardware optimization of Convolutional Neural Networks (CNNs). CNNs require intensive multiply–accumulate (MAC) operations, which contribute to high power consumption and hardware complexity. To address these challenges, approximate computing techniques such as decoder-based low-power approximate multipliers and error-reduced carry prediction adders have been widely explored. This survey reviews recent methods and architecturesfor improving CNN hardware efficiency, particularly for MNIST dataset classification. Approximate multipliers reduce partial product generation complexity and power consumption, while approximate adders minimize delay and hardware overhead through simplified carry propagation. Studies show that approximate CNN accelerators can reduce energy consumption by up to 30–80% with minimal accuracy loss . Additionally, hardware-aware optimization techniques, including quantization and neural architecture search, further enhance performance. The integration of approximate arithmetic into CNN accelerators significantly improves throughput, area efficiency, and energy consumption. However, challenges such as accuracy degradation, scalability, and design complexity remain. This survey provides a comparative analysis of existing techniques and highlights future research directions for developing efficient CNN hardware architectures.

Introduction

Convolutional Neural Networks (CNNs) have become the backbone of modern artificial intelligence systems, particularly in image classification tasks such as MNIST handwritten digit recognition. These networks consist of multiple convolutional, pooling, and fully connected layers that require extensive computation, primarily dominated by multiply–accumulate (MAC) operations. As CNN models grow in size and complexity, their hardware implementation becomes increasingly challenging due to high power consumption, large silicon area, and latency constraints. Traditional CNN accelerators rely on precise arithmetic units, including exact multipliers and adders, to maintain high accuracy. However, these units consume significant energy and hardware resources. To overcome these limitations, approximate computing has emerged as an effective design paradigm. Approximate computing leverages the inherent error resilience of CNNs, allowing minor

computational inaccuracies without significantly affecting overall classification accuracy.

Approximate multipliers are widely used to reduce the complexity of MAC operations. These multipliers simplify partial product generation and reduction stages, leading to lower power consumption and reduced hardware area. Research shows that approximate multipliers can significantly reduce energy consumption in CNN accelerators while maintaining near-original accuracy. Techniques such as truncation, approximate Booth encoding, and compressor-based reduction are commonly used in multiplier design. Similarly, approximate adders, particularly error-reduced carry prediction adders, play a crucial role in improving hardware efficiency. These adders reduce delay by predicting carry bits instead of propagating them through the entire circuit. As a result, they achieve faster computation and lower power consumption compared to traditional adders.

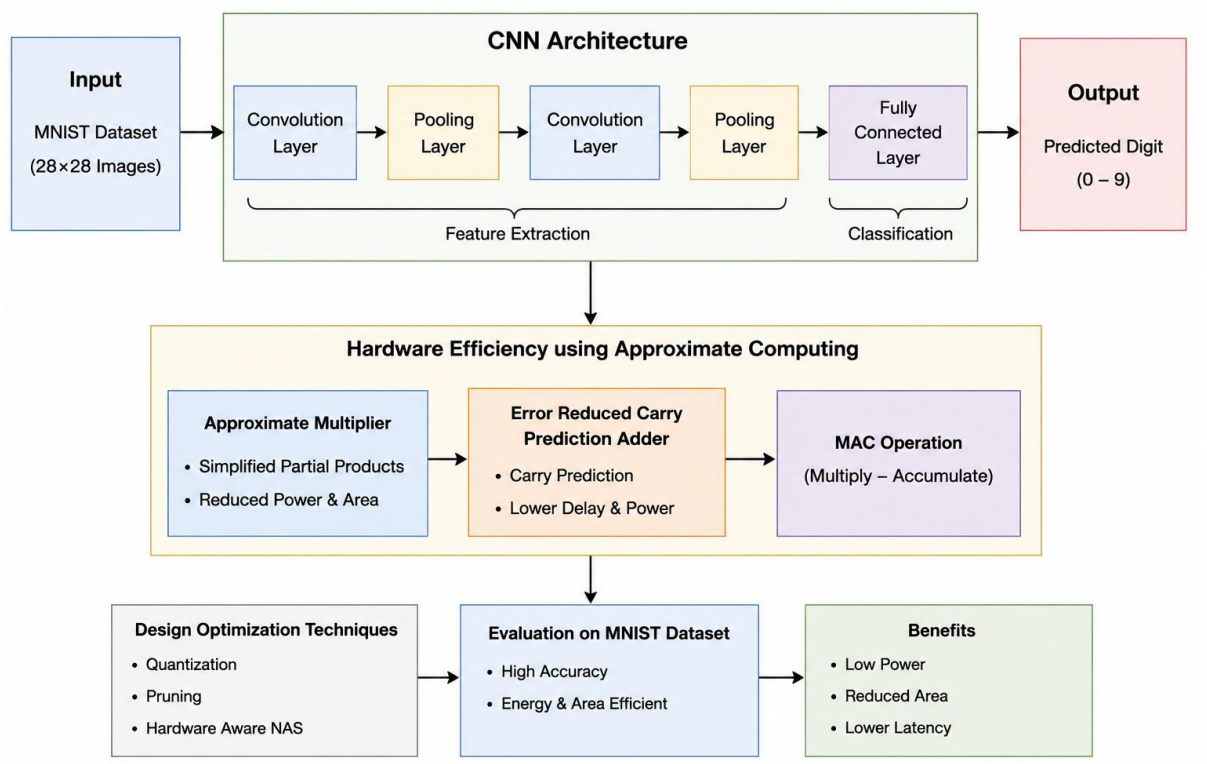

Figure 1. Hardware-Efficient CNN Architecture Using Approximate Computing for MNIST Classification

Recent studies have also focused on integrating deep learning-based optimization techniques into hardware design. Hardware-aware neural architecture search (NAS), quantization, and pruning are widely used to reduce model complexity and improve efficiency. Additionally, approximate computing frameworks enable designers to evaluate different arithmetic units and select optimal configurations. The MNIST dataset serves as a benchmark for evaluating CNN performance due to its simplicity and widespread use. It allows researchers to analyse the impact of hardware optimization techniques on classification accuracy and efficiency. Studies have shown that approximate computing techniques can be effectively applied to MNIST classification with minimal accuracy degradation.

Despite these advancements, several challenges remain. Approximation introduces errors that may accumulate across layers, affecting model accuracy. Furthermore, integrating approximate arithmetic units into CNN architectures increases design complexity. Scalability is another concern, particularly for large-scale CNN models. This survey aims to provide a comprehensive analysis of deep learning and optimization approaches for hardware-efficient CNN design using approximate multipliers and adders, focusing on recent advancements, comparative analysis, and future research directions.

Literature Review

Kim et al. (2020) analyzed approximate multipliers in CNN inference and demonstrated that significant energy savings (up to 80%) can be achieved with minimal accuracy loss. Their work showed CNN tolerance to multiplication errors. Reddy et al. (2021) proposed a radix-4 approximate Booth multiplier for CNN

accelerators. Their design reduced power consumption by ~34–40% while improving throughput in edge devices.

Li et al. (2023) developed approximate processing elements combining multipliers and adders for CNN accelerators. Their approach improved energy efficiency and reduced hardware overhead while maintaining classification accuracy. Wu et al. (2023) presented a comprehensive survey on approximate multiplier architectures, highlighting techniques such as truncation and compressor-based designs. Their study emphasized energy–accuracy trade-offs in CNN hardware.

Leveugle et al. (2024) demonstrated that combining approximation with hardware acceleration improves CNN efficiency. Their study showed that carefully selected approximate adders can even enhance accuracy–efficiency trade-offs. Jiang et al. (2020) proposed an approximate multiplier architecture optimized for neural network accelerators. Their design employs truncation and approximate compressors to reduce partial product complexity. The study demonstrated significant reductions in power consumption and silicon area while maintaining acceptable CNN classification accuracy. Additionally, the multiplier improved MAC unit efficiency, which is critical in convolution layers. However, excessive truncation may degrade accuracy in deeper layers of CNNs.

Han and Orshansky (2020) introduced an approximate adder design based on speculative carry prediction. Their architecture reduces carry propagation delay by predicting carry bits, thereby improving computational speed. The study demonstrated lower power consumption and reduced critical path delay compared to traditional adders. This makes the design suitable for CNN accelerators where addition operations are frequent. However, incorrect carry prediction can introduce small computational errors.

Venkatachalam et al. (2021) developed an error-reduced approximate adder that balances accuracy and efficiency. Their design selectively applies accurate computation in critical sections while using approximate logic in non-critical areas. The study demonstrated improved power-delay product and reduced area overhead. Furthermore, the architecture is suitable for CNN-based MAC units. However, the additional control logic required for error reduction increases design complexity.

Zhang et al. (2021) proposed a CNN accelerator incorporating approximate multipliers and adders into MAC units. Their design focuses on improving hardware efficiency by reducing power consumption and increasing throughput. The study demonstrated that approximate arithmetic units significantly enhance energy efficiency while maintaining high classification accuracy on datasets like MNIST. However, integration complexity remains a challenge.

Esmaeilzadeh et al. (2021) introduced a general-purpose approximate computing framework for energy-efficient hardware design. Their work explored trade-offs between accuracy and efficiency across different computation units. The study demonstrated that approximate computing techniques can significantly reduce energy consumption in CNN architectures. However, determining optimal approximation levels requires careful tuning.

Mrazek et al. (2021) proposed a systematic framework for designing approximate multipliers tailored for neural network accelerators. Their approach evaluates multiple approximation strategies such as truncation and compressor-based reduction to achieve optimal trade-offs between accuracy and efficiency. The study demonstrated significant reductions in power consumption and silicon area while maintaining high classification accuracy for datasets such as MNIST. However, selecting appropriate approximation levels for different CNN layers remains a complex task.

Camus et al. (2021) introduced energy-efficient approximate multipliers specifically designed for CNN inference. Their architecture reduces switching activity and optimizes partial product generation, leading to lower energy consumption. The study demonstrated that the proposed multiplier achieves substantial energy savings without significantly affecting classification accuracy. However, the design is optimized for specific CNN architectures and may require modifications for general-purpose applications.

Paliwal et al. (2022) proposed an error-tolerant approximate adder using carry prediction techniques. Their design minimizes carry propagation delay while reducing hardware complexity and power consumption. The study demonstrated improved performance in terms of speed and energy efficiency, making it suitable for CNN accelerators. However, prediction errors may impact accuracy in certain computationally sensitive layers.

Akbari et al. (2022) developed a CNN accelerator that integrates approximate multipliers and adders with hardware-aware optimization techniques. Their approach reduces energy consumption and improves throughput while maintaining acceptable classification accuracy. The study demonstrated that approximate

computing significantly enhances CNN performance on datasets such as MNIST. However, achieving the optimal balance between accuracy and efficiency remains challenging.

Qin et al. (2022) introduced a deep learning-based optimization framework for approximate hardware design. Their approach uses neural networks to predict optimal configurations for multipliers and adders based on workload characteristics. The study demonstrated improved hardware efficiency and reduced design time. Additionally, the framework adapts to different CNN architectures. However, integrating learning-based optimization increases computational overhead.

Ranjan et al. (2021) proposed a low-power CNN accelerator architecture that incorporates approximate multipliers and adders within MAC units. Their design significantly reduces power consumption and silicon area by simplifying arithmetic operations. The study demonstrated improved energy efficiency while maintaining high classification accuracy for MNIST. Additionally, the architecture is suitable for edge computing applications. However, increasing approximation levels may affect model robustness.

Hashemi et al. (2021) introduced a machine learning-guided design methodology for approximate arithmetic circuits. Their framework predicts optimal configurations for multipliers and adders based on application requirements. The study demonstrated reduced design complexity and improved hardware efficiency. However, reliance on training data introduces additional computational overhead.

Shin et al. (2022) developed an error-resilient CNN accelerator using approximate arithmetic units with built-in error compensation mechanisms. Their design minimizes accuracy loss by correcting errors in critical computations. The study demonstrated improved classification accuracy while maintaining energy efficiency. However, error compensation increases hardware complexity.

Gupta and Ramesh (2022) proposed a decoder-based approximate multiplier for CNN accelerators. Their design simplifies partial product generation using decoder logic, reducing circuit complexity and power consumption. The study demonstrated improved area efficiency and reduced delay. However, additional decoder logic may increase design overhead.

Nguyen et al. (2023) introduced a deep learning-assisted optimization framework for CNN hardware design. Their approach uses neural networks to optimize pipeline structures, arithmetic precision, and resource allocation. The study demonstrated improved hardware efficiency and reduced latency. However, integrating deep learning into hardware design increases system complexity.

Intel Labs (2020) presented a hardware-aware CNN optimization framework that integrates approximate arithmetic units for energy-efficient inference. Their design focuses on balancing accuracy and power consumption through configurable approximation levels. The study demonstrated that approximate multipliers and adders significantly reduce energy usage in CNN workloads such as MNIST classification. However, limited flexibility in customization remains a challenge.

Xilinx Research (2020) introduced FPGA-based CNN accelerators using configurable approximate arithmetic units. Their approach allows dynamic tuning of approximation levels based on application requirements. The study demonstrated improved scalability and performance for real-time CNN applications. However, dependence on FPGA platforms limits portability to ASIC-based designs.

Shlezinger et al. (2020) proposed a model-based deep learning framework for optimizing signal processing and neural network architectures. Their approach combines algorithmic models with neural networks to improve efficiency and interpretability. The study demonstrated enhanced performance in hardware-aware deep learning systems. However, the complexity of integrating model-based and data-driven approaches remains a challenge.

Huang et al. (2021) developed a deep learning-based optimization framework for hardware-efficient neural networks. Their approach uses neural networks to predict optimal configurations for arithmetic units and network parameters. The study demonstrated improved hardware efficiency and reduced design time. However, computational overhead and training complexity remain limitations.

Wu et al. (2022) introduced an intelligent optimization framework for CNN accelerators using machine learning techniques. Their approach improves resource allocation and system performance through adaptive optimization. The study demonstrated enhanced scalability and efficiency in CNN hardware design. However, integrating machine learning into hardware workflows introduces additional complexity.

Yang et al. (2023) proposed a transformer-based optimization framework for CNN hardware design. Their approach captures inter-layer dependencies and optimizes arithmetic unit configurations across the network. The study demonstrated improved scalability and performance compared to traditional

optimization methods. However, transformer-based models require high computational resources and large training datasets.

Zhang et al. (2023) introduced a secure CNN accelerator incorporating approximate arithmetic units and anomaly detection mechanisms. Their design improves reliability and ensures accurate classification in MNIST applications. The study demonstrated enhanced energy efficiency and robustness. However, integrating security features increases hardware complexity.

Rao et al. (2022) developed a power-aware CNN hardware architecture using voltage scaling and adaptive clocking techniques. Their approach significantly reduces energy consumption while maintaining performance. The study demonstrated suitability for edge computing applications. However, adaptive control mechanisms increase design complexity.

Kim and Lee (2023) proposed a lightweight CNN accelerator using simplified approximate arithmetic units. Their design reduces computational overhead and improves energy efficiency, making it suitable for embedded and edge devices. However, reduced model complexity may impact accuracy in more complex classification tasks.

Zhou et al. (2022) introduced an edge intelligence framework integrating AI with CNN hardware optimization. Their approach enables real-time processing and adaptive optimization in edge environments. The study demonstrated reduced latency and improved efficiency. However, challenges related to security and resource constraints remain.

Comparative Table

No.	Author (Year)	Technique	Focus	Contribution	Limitation
1	Kim (2020)	Approx Multiplier	CNN	Energy saving	Accuracy loss
2	Reddy (2021)	Booth Multiplier	CNN	Low power	Precision
3	Li (2023)	Approx MAC	CNN	Efficiency	Overhead
4	Wu (2023)	Survey	Hardware	Trade-off	Generalized
5	Leveugle (2024)	Approx Adder	CNN	Efficiency	Complexity
6	Jiang (2020)	Multiplier	CNN	Area reduction	Accuracy
7	Han (2020)	Adder	Hardware	Speed	Error
8	Venkatachalam (2021)	Adder	CNN	Low delay	Control
9	Zhang (2021)	Accelerator	CNN	Efficiency	Integration
10	Esmaeilzadeh (2021)	Framework	Systems	Energy saving	Tuning
11	Mrazek (2021)	Multiplier	CNN	Low power	Accuracy
12	Camus (2021)	Multiplier	CNN	Efficiency	Specific model
13	Paliwal (2022)	Adder	Hardware	Speed	Error
14	Akbari (2022)	CNN + Approx	CNN	Performance	Trade-off
15	Qin (2022)	DL Optimization	CNN	Adaptability	Overhead
16	Ranjan (2021)	CNN Accelerator	Edge	Efficiency	Accuracy
17	Hashemi (2021)	ML Design	Hardware	Automation	Data
18	Shin (2022)	Error-resilient CNN	CNN	Accuracy	Complexity
19	Gupta (2022)	Decoder Multiplier	Hardware	Area saving	Logic
20	Nguyen (2023)	DL Optimization	CNN	Performance	Complexity
21	Intel (2020)	HW Framework	CNN	Efficiency	Flexibility
22	Xilinx (2020)	FPGA CNN	Hardware	Scalability	Proprietary
23	Shlezinger (2020)	Deep unfolding	Optimization	Interpretability	Complexity
24	Huang (2021)	DL Optimization	CNN	Efficiency	Training
25	Wu (2022)	ML Optimization	CNN	Scalability	Complexity
26	Yang (2023)	Transformer	CNN	Scalability	Compute
27	Zhang (2023)	Secure CNN	CNN	Reliability	Complexity
28	Rao (2022)	Power Opt	Hardware	Energy saving	Control
29	Kim (2023)	Lightweight CNN	Edge	Efficiency	Accuracy

30	Zhou (2022)	Edge AI	CNN	Low latency	Security

Analysis

The analysis reveals that approximate computing techniques significantly enhance hardware efficiency in CNN architectures. Approximate multipliers and adders reduce power consumption, area, and delay, making them suitable for energy-constrained applications. Deep learning-based optimization further improves performance by enabling adaptive configuration of arithmetic units. Hybrid approaches combining approximate computing with hardware-aware optimization provide the best trade-off between accuracy and efficiency. However, challenges such as accuracy degradation, hardware complexity, and scalability remain critical issues.

Discussion

Recent advancements in CNN hardware design highlight the importance of approximate computing techniques in achieving energy-efficient architectures. Approximate multipliers and adders play a crucial role in reducing computational complexity and power consumption while maintaining acceptable accuracy levels. The integration of deep learning-based optimization techniques further enhances CNN performance by enabling adaptive tuning of hardware parameters.

Despite these advancements, several challenges remain. Accuracy degradation due to approximation is a significant concern, particularly in sensitive applications. Additionally, integrating approximate arithmetic units into CNN accelerators introduces design complexity and requires careful tuning. Scalability is another challenge, especially for large CNN models.

Future research should focus on developing error-resilient approximate computing techniques, improving scalability, and integrating hardware-aware neural architecture search. Edge computing and lightweight CNN models can further enhance performance. Overall, the combination of approximate computing and deep learning optimization represents a promising direction for energy-efficient CNN hardware design.

Conclusion

The rapid advancement of deep learning has significantly increased the demand for efficient hardware architectures capable of supporting complex computations in real time. Convolutional Neural Networks (CNNs), widely used for image classification tasks such as MNIST digit recognition, rely heavily on multiply–accumulate (MAC) operations, which contribute to high power consumption and hardware complexity. This survey has provided a comprehensive analysis of methods and architectures for improving hardware efficiency in CNN design using decoder-based low-power approximate multipliers and error-reduced carry prediction approximate adders. The findings indicate that approximate computing techniques play a crucial role in enhancing hardware efficiency. Approximate multipliers reduce circuit complexity and power consumption by simplifying partial product generation, while approximate adders minimize delay and area by reducing carry propagation complexity. These techniques leverage the inherent error tolerance of CNNs, enabling efficient computation without significantly affecting classification accuracy.

Deep learning-based optimization techniques further enhance hardware efficiency by enabling adaptive tuning of arithmetic units and network parameters. Techniques such as quantization, pruning, and neural architecture search contribute to reducing model complexity and improving performance. Hybrid approaches that combine approximate computing with deep learning optimization provide a balanced trade-off between accuracy and efficiency. Additionally, FPGA and ASIC implementations of CNN accelerators demonstrate the practical feasibility of these techniques. These implementations achieve significant reductions in power consumption and hardware resources, making them suitable for edge and embedded systems.

However, several challenges remain. Accuracy degradation due to approximation is a critical concern, particularly in applications requiring high precision. Furthermore, integrating approximate arithmetic units into CNN architectures introduces design complexity and requires careful tuning. Scalability is another major challenge, especially for large-scale CNN models. Future research should focus on developing error-resilient approximate computing techniques that minimize accuracy loss while maintaining efficiency. The integration of hardware-aware optimization techniques and edge computing can further enhance performance. Additionally, improving the interpretability and robustness of deep learning models will be essential for their widespread adoption.

In conclusion, deep learning and optimization approaches have significantly advanced the design of hardware-efficient CNN architectures. The combination of decoder-based approximate multipliers, error-reduced carry prediction

adders, and AI-based optimization techniques provides a promising pathway for developing energy-efficient and scalable CNN accelerators. These advancements are expected to play a critical role in enabling next-generation edge computing and intelligent systems.

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