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FFT IMPLEMENTATION BY FPGA USING VEDIC MATHEMATICS

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Abstract: *Fast Fourier Transform is important data processing technique in communication systems and DSP systems. In this, we propose high speed and area efficient 8 point FFT processor using Vedic algorithm. For the reduction of computational complexity and area, we develop FFT architecture by designing a radix-4 algorithm and optimizing the realization by Vedic algorithm. Moreover, the design achieves very high speed, which makes them suitable for the most demanding applications of FFT. The proposed radix-4 Vedic algorithm based architecture requires lesser hardware resources. The synthesis results are same as that of theoretical analysis and it is observed that more than 15% reduction can be achieved in terms of slices count. In addition, the dynamic power consumption can be reduced and speed can be increased by as much as 16% using Vedic algorithm.*

Keywords *- FFT, Vedic algorithm, radix-4.*

1. INTRODUCTION

Now days, Orthogonal Frequency Division Multiplexing (OFDM) is one of the most important application of Fast Fourier Transform (FFT). It is mainly used in wireless local area network (WLAN), digital audio broadcasting (DAB), digital video broadcasting-terrestrial (DVB-T) and digital video broadcasting-handheld (DVB-H). The FFT is a faster version of the Discrete Fourier Transform (DFT) and calculates Discrete Fourier Transform efficiently in our work by reducing the computational complexity. Memory-based architecture consisting of butterfly processing element and memory units has been widely adapted to design FFT processor. It utilizes less power but high latency and fewer throughputs. To increase the efficiency of memory based FFT architecture, radix-4 butterfly processing units along with dual port memory is used.

Fast Fourier Transform (FFT) is widely used in the field of digital signal processing (DSP) and communication system applications with the advancement of VLSI. The cost and

characteristic of FFT processor is decided by butterfly processing unit which consists of complex adders and multipliers. The multiplier usually increases the speed of the FFT processor. Usage of complex multiplications using shift and add operation results in higher hardware cost and also limits the performance of FFT. To improve the performance of such complex calculations Vedic algorithm is used. Vedic algorithm gives efficient implementation of complex multiplier.

VEDIC mathematics is an ancient Indian system of mathematics which mainly deals with Vedic mathematical formulae and their applications. The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. Vedic mathematics was reconstructed from the ancient Indian scrip-tures (Vedas) by Sri Bharati Krisna Tirtha (1884-1960) after his eight years of research on Vedas. In this we are using Vedic multiplier architecture based on the ancient Vedic mathematics Sutra (formula) called Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra which was traditionally used for decimal system in ancient India. In this Sutra, it is shown to be a much more efficient multiplication algorithm as compared to the conventional counter parts. Urdhva-Tiryakbhyam Sutra is firstly applied to the binary number system and is used to develop digital multiplier architecture. The effectiveness of reducing the N×N multiplier structure into an efficient 4×4 multiplier structures has been done by this sutra. This work presents a systematic design methodology for fast and area efficient digital multiplier based on Vedic mathematics.

In recent years, various researches have been done in the design of multi-path pipelined FFT processors that provide a high throughput. The area became even larger because of the memory modules being duplicated for the 16 data path approach. To reduce the area and power consumption, several FFT algorithms and dynamic scaling schemes were proposed. The radix of the algorithm greatly affects the architecture of the FFT processor and the complexity of the implementation. A high radix reduces the number of twiddle factor multiplications. The radix r_k algorithms simultaneously achieve a simple butterfly and a reduced number of twiddle factor multiplications

2. LITERATURE SURVEY

Due to the advancement in multimedia and wireless communication, now a day's digital signal processing has received high attention. The Fast Fourier Transform (FFT) is reckoning intensive digital signal processing (DSP) function mostly used in applications such as image processing, software-defined radio, wireless communication, instrumentation. The FFT has been designed, optimized and implemented on an FPGA based system. Hence utilization of area efficient as well as high speed multipliers and adders in Fast Fourier Transform will give enhanced accomplishment and efficiency. In this paper, design of FFT using Vedic multiplier with high speed and small area has been presented. To perform fast and complex arithmetic functions one of the fastest adders called Carry Select Adders (CSLA) are used. The coding of the FFT processor based on Vedic mathematics is done in VHDL (very high speed integrated circuit hardware description language) and synthesis is done using Xilinx ISE series. In this paper, high speed and area efficient 8 point FFT processor using Vedic algorithm has been proposed. The ancient Indian system of mathematics, Vedic mathematics was rediscovered in early twentieth century. Vedic mathematics is based on sixteen principles or word-formulae which are termed as Sutras. The similarity of the popular array multiplier is presented and is shown using the hardware

architecture of the Vedic multiplier. One of the fastest and low power multipliers are based on Vedic mathematics. By enabling parallel generation of partial product it eliminates unwanted multiplication steps. Thus Vedic multipliers significantly reduce the propagation delay in FFT processor. Vedic multiplier reduces hardware complexity in area and number of cells in FPGA implementation. The proposed processor has been designed in Xilinx and implemented using Spartan 3A FPGA kit. Urdhava Tiryakbhyam algorithm of Vedic Mathematics is used to improve its efficiency. Urdhva Tiryakbhyam is one of the oldest Indian Vedic sutra which deals with multiplication and completely eliminates unwanted multiplication steps. After a gentle introduction of this Sutra, this algorithm is applied to the binary number system making it useful in the digital hardware.

3. DESCRIPTION OF TECHNOLOGIES USED

3.1. FFT (Fast Fourier Transform)

Fast Fourier Transform (FFT) is the one of the fundamental operations that is typically performed in any DSP system. Basic formula of computation of FFT is

$$\mathbf{X(k) = WNnk \quad 0 \leq k \leq N\text{-}1}$$

The Fast Fourier Transform (FFT) is a computationally intensive digital signal processing (DSP) function widely used in applications such as imaging, software-defined radio, wireless communication, instrumentation and machine inspection.

3.2. Vedic Algorithm

Vedic mathematics is the ancient Indian system of mathematics. It mainly deals with Vedic mathematical formulae and their application to various branches of mathematics. The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krsna Tirtha (1884-1960). According to the research made by him, Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as Sutras. The beauty of Vedic mathematics lies in the fact that it reduces otherwise cumbersome looking calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

3.3. RADIX-4

An efficient class of radix algorithm for designing FFT is radix-4 algorithm. In radix-4 algorithm, there are $\log_4 N$ stages and each stage has N/4 4-point butterflies. The radix-4 algorithm operates by decomposing N point input data sequence into N/4 different points. The radix-4 algorithm can be defined by (4)

Where, $\mathbf{k=0,1,\ldots(N/4)\text{-}1,\ m=0,1,2,3}$

The N-point FFT can be decomposed to repeat micro operations called butterfly operations. When the dimension of the butterfly is r, the FFT operation is called a radix-r FFT. For FFT hardware realization, if only one butterfly structure is enforced in the chip, this butterfly unit will execute all the calculations recursively. This indicates that a radix-4 FFT can be four times faster than a radix-2 FFT. The total number of complex multiplication is (3N/4) and the

number of required complex additions is (3N/4). Thus, radix-4 algorithm reduces number of complex multiplier.

4. PROPOSED ARCHITECTURE

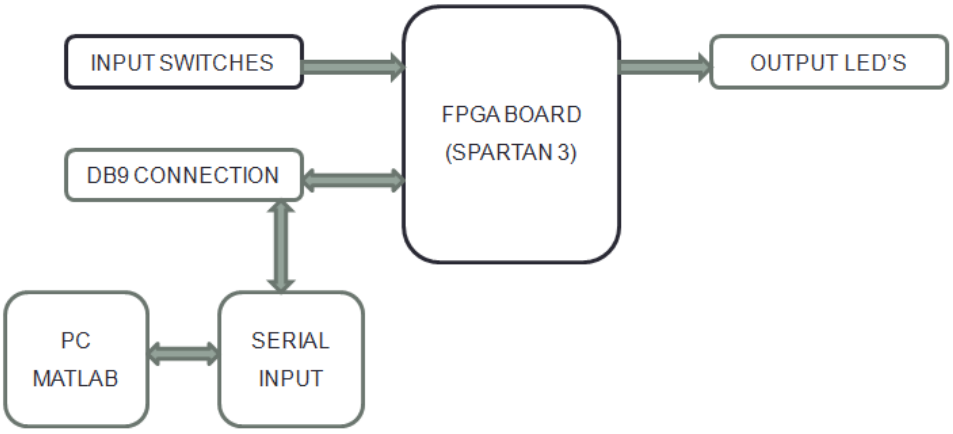

Fig.1: Proposed diagram of 8-point FFT using VEDIC algorithm

5. ADVANTAGES OF PROPOSED SYSTEM

- Orthogonal Frequency Division Multiplication Systems (OFDM)
- Digital Signal Processing Systems (DSP)
- Communication Systems

6. RESULT AND DISSCUSION

SYNTHESIS RESULT	
No. of Slices	14 out of 704(1%)
No. of LUT's	25 out of 1408(1%)
No. of I/O Blocks	16
Max. Combinational Path Delay (ns)	20.299
Levels of Logic	15

Table.1: Synthesis result

Comparison of Conventional Multiplier and VEDIC Multiplier

SrNo	Multiplier Type	No. of Slices	No. of LUT's	No. of I/O Blocks	Max. Combinational Path Delay (ns)	Levels of Logic
1.	Conventional Multiplier	154 out of 704(21%)	273 out of 1408(19%)	32	23.707	19

2.	VEDIC Multiplier	14 out of 704(1%)	25 out of 1408(1%)	16	20.299	15

Table.2: Comparison of Conventional Multiplier and VEDIC Multiplier on Spartan 3s500eft256-5

SYNTHESIS RESULT: Following Table1. Shows the synthesis result for implementation of FFT processor using VEDIC mathematics. The Table 2. Shows the comparison between the conventional multiplier and VEDIC multiplier. In this way, the proposed architecture provides the useful implementation of VEDIC multiplier in real time applications.

7. CONCLUSION

In this paper, a new radix-4 FFT processor suitable for OFDM system has been proposed. High operation speed by employing several performance-enhancement techniques, including a recursive use of radix-4 algorithm realized with multiple memory banks, a conflict-free memory addressing scheme, and a new Vedic multiplier based twiddle factor multiplier structure has been proposed by this architecture. Also, area minimization is obtained by devising an efficient Vedic algorithm based butterfly processing structure, while the novel twiddle factor multiplier has low power consumption and hardware complexity. Synthesis results show that the proposed FFT processor can provide up to 20.299 speed and slices count is 14 out of 704(1%).The proposed FFT architecture can also be altered to support other longer FFT sizes.

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