



Design and Development of a Microcontroller-Based Automatic Power Factor Correction System

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Abstract

Low power factor caused by inductive loads increases line current, conductor losses, voltage drop, and the apparent-power demand of electrical installations. This methodology paper presents the design and development of a low-cost automatic power factor correction (APFC) system in which a microcontroller continuously estimates the phase displacement between voltage and current and switches a stepped shunt-capacitor bank to maintain the power factor near a selected target. The proposed hardware uses isolated voltage and current sensing, zero-crossing detectors, a PIC16F877A microcontroller, a ULN2003A relay driver, electromechanical relays, a 5/10/20/40 μF capacitor bank, and a 16 $\times$ 2 display. The control method calculates power factor from the zero-crossing time difference, estimates the required reactive-power compensation, selects the closest capacitor combination, and applies hysteresis and switching delay to prevent relay hunting. Design verification is performed for representative 230 V, 50 Hz inductive loads rather than being presented as a field trial. Analytical validation indicates that typical initial power factors between 0.62 and 0.81 can be raised to approximately 0.94–0.99 with corresponding line-current reductions of about 15–37%. The methodology emphasizes electrical isolation, capacitor discharge, conservative switching, and calibration so that the design can be reproduced in an educational or small-load laboratory environment.

Introduction

Power factor (PF) expresses how effectively apparent power supplied by an alternating-current source is converted into useful active power. For a near-sinusoidal single-phase load, PF is approximately the cosine of the phase angle between voltage and current. Induction motors, transformers, fluorescent-ballast circuits, and many electromagnetic devices draw magnetizing reactive current, producing a lagging power factor. The resulting increase in rms line current raises I^2R losses and voltage drop and reduces the usable capacity of conductors, transformers, and switchgear. Early adaptive compensation research demonstrated that dynamically controlled reactive-power support can improve

the operating condition of induction-generator systems [10], while later work on line conditioning and digitally controlled power-factor correction showed the practical value of fast electronic control [9].

For fixed loads, a properly sized shunt capacitor can compensate part of the inductive reactive power. The difficulty appears when the load varies: a fixed capacitor may under-compensate during heavy loading or over-compensate at light loading. Automatic switching therefore becomes important. Microcontroller-based systems are attractive because timing capture, threshold logic, capacitor-step selection, display functions, and fault interlocks can be implemented in one

low-cost controller. Barsoum [6] described PIC-based measurement and switching for power-factor correction, and subsequent implementations used microcontrollers to measure the phase relation and connect capacitor groups according to the required compensation [4]. Arduino-based work similarly showed that a zero-crossing approach can provide a simple automatic single-phase controller for inductive loads [3].

By 2017, several practical APFC studies had combined current and voltage sensing, zero-crossing conversion, embedded control, relay drivers, and capacitor banks. Goyal et al. [1] calculated the phase difference from the time separation of voltage and current crossings and used the resulting PF to control relay-selected capacitors. Hirave et al. [2] incorporated PIC-based monitoring and correction and emphasized continuous observation of electrical variables. These studies motivate the present methodology, but the design here is organized as a reproducible engineering procedure with explicit capacitor sizing, switching logic, hysteresis, calibration, and verification criteria. The objective is not to claim a new compensation principle; it is to provide a clear methodology for designing and evaluating an APFC prototype whose components and control logic are appropriate to the technology available up to 2017.

Literature Review

Research on automatic power-factor control evolved from adaptive reactive-power compensation toward embedded and intelligent controllers. El-Sharkawi et al. [10] proposed an adaptive PF controller for three-phase induction generators, establishing the importance of matching compensation to operating conditions rather than relying only on fixed correction. Kim et al. [9] later developed a high-performance line conditioner combining voltage regulation and PF correction, illustrating that power-quality objectives can be coordinated through controlled conversion. Although those systems differ from a relay-switched capacitor bank, both works provide the control-system foundation: measurement, decision, and controlled reactive-power intervention.

Embedded implementation became more

accessible with low-cost microcontrollers. Barsoum [6] used a PIC microcontroller to determine PF and trigger sufficient capacitive compensation, demonstrating that a compact digital controller can replace manual switching. Sagioglu, Colak, and Bayindir [8] embedded an artificial-neural-network compensator in a PIC16F877 for fast reactive-power control, while Bayindir, Sagioglu, and Colak [5] further developed an intelligent PF corrector using neural-network techniques. These intelligent approaches reduced delay and over/under-compensation, but their computational and commissioning requirements can be unnecessary for small educational or workshop loads where a deterministic stepped bank is adequate.

A closely related microcontroller application by Azcondo et al. [7] used digital control in a PF-correction stage for high-intensity-discharge lamp ballast, reinforcing the suitability of embedded controllers for real-time PF-oriented decisions. Nagarajan and Kandasamy [4] presented an optimal PF-correction scheme for inductive loads using PIC-based sensing and switched capacitors. Ishak et al. [3] implemented an automatic single-phase controller using an Arduino Uno/ATmega328, voltage and current transformers, and zero-crossing detectors, with correction initiated when PF fell below the selected value. These studies are especially relevant to the present topology because they combine low-cost sensors, timing-based PF estimation, and discrete capacitor switching.

The 2017 studies of Goyal et al. [1] and Hirave et al. [2] show the maturity of the basic APFC architecture: sensing circuits condition the mains waveforms, zero-crossing detectors translate them into logic transitions, the controller measures the time displacement, and relays insert capacitor steps. The remaining methodological issues are not the existence of the architecture but the rigor of design decisions—how the target PF is selected, how capacitor values are calculated, how over-compensation is avoided, how switching transients and relay chatter are reduced, and how calibration error affects the decision boundary. The proposed methodology therefore adopts the proven architecture while making these design steps explicit.

Table 1. Summary of literature used to define the proposed APFC methodology.

Ref.	Year	Control Hardware	Main contribution	Relevance to this work
[10]	1985	Adaptive controller	Dynamic PF control for induction generators	Motivates adaptive compensation

[9]	2004	Controlled line conditioner	Combined PF correction and voltage regulation	Shows coordinated power-quality control
[8]	2006	PIC + ANN	Fast intelligent reactive-power compensation	Supports embedded decision control
[6]	2007	PIC microcontroller	PF sensing and capacitor switching	Direct basis for microcontroller APFC
[5]	2009	ANN-based corrector	Intelligent PF control under variable loads	Highlights response and accuracy
[4]	2012	PIC + capacitor bank	Optimized correction for inductive load	Supports capacitor-step selection
[3]	2015	Arduino + ZCD	Automatic single-phase PF controller	Supports simple timing-based sensing
[1],[2]	2017	PIC / relay bank	Monitoring and practical APFC implementation	Provides recent pre-2018 benchmark

Collectively, the literature indicates that a useful low-cost APFC design should include isolated sensing, deterministic phase measurement, a defined capacitor-selection rule, a stable switching policy, and visible feedback to the operator. The present work follows these principles and intentionally avoids references later than 2017, as required for the scope of this paper.

Methodology

1. System Requirement Definition

The proposed system is designed for a laboratory-scale, single-phase 230 V, 50 Hz

supply feeding variable inductive loads. The correction target is $PF \geq 0.95$, with an upper control band near 0.99 to avoid excessive leading compensation. The controller must measure phase displacement, display PF, select capacitor steps automatically, and disconnect the bank when the load is absent or when the sensed condition is invalid. The design philosophy follows the timing-based APFC method reported in [1], [3], [4], and [6], but adds explicit hysteresis and a minimum dwell time between switching events.

2. Functional Architecture

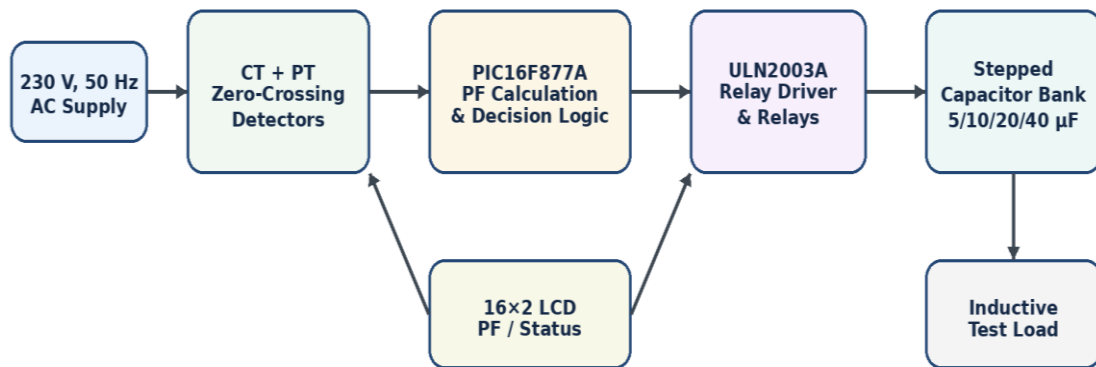


Figure 1. Block diagram of the proposed microcontroller-based APFC system.

A small potential transformer (PT) and current transformer (CT) provide galvanically isolated representations of line voltage and current. Comparator-based zero-crossing detector (ZCD) circuits convert the sensed sinusoidal waveforms into logic pulses. The PIC16F877A receives the two pulse trains at interrupt-capable pins and uses an internal timer to determine the crossing-time difference. A ULN2003A transistor-array driver energizes relay coils, while each relay connects one capacitor step in parallel with the load. The LCD reports measured PF, the selected capacitance, and correction status. The sensing

and control arrangement is consistent with the embedded APFC structures described by Goyal et al. [1] and Hirave et al. [2].

3. Power-Factor Measurement

For a sinusoidal supply, the phase angle is obtained from the time difference Δt between equivalent voltage and current zero crossings. At supply frequency f , the phase angle in degrees is:

$$\varphi = 360 f \Delta t$$

The displacement power factor is then calculated as:

$$PF = \cos(\varphi)$$

At 50 Hz one electrical cycle is 20 ms, so a 1 ms time displacement corresponds to 18°. The firmware averages several consecutive measurements to reduce timing jitter and rejects pulses outside a physically plausible window. A calibration offset, measured using a resistive load with PF close to unity, is subtracted from Δt to account for unequal delays in the CT/PT and comparator channels. This calibration is important because even small sensing delays can bias the decision near the 0.95 threshold.

4. Reactive-Power and Capacitor Sizing

If active power P is known or estimated and the initial and desired power factors are PF_1 and PF_2 , the required capacitive reactive power Q_c is determined by the standard compensation relation:

$$Q_c = P [\tan(\cos^{-1} PF_1) - \tan(\cos^{-1} PF_2)]$$

For a shunt capacitor operating at rms voltage V and angular frequency $\omega = 2\pi f$, the corresponding capacitance is:

$$C = Q_c / (2\pi f V^2)$$

A binary-like four-step bank of 5, 10, 20, and 40 μF was selected, giving correction values from 5 to 75 μF in 5 μF increments. Each capacitor must be an AC-rated power-factor-correction or motor-run capacitor suitable for the applied voltage, and each branch requires appropriate protection and a discharge resistor. The step size is intentionally modest because small increments reduce the risk of overshooting the target PF. Capacitor selection follows the same reactive-power principle used in PIC-based APFC research [4], while the discrete switching arrangement is consistent with the low-cost controller approach of [3] and [6].

Table 2. Proposed hardware specification for the APFC prototype.

Subsystem	Selected element	Design role / criterion
Controller	PIC16F877A	Timer/interrupt capture, PF calculation, relay logic, LCD control
Voltage sensing	230/6–9 V isolated PT + ZCD	Safe phase reference; calibrated zero-crossing pulse
Current sensing	CT + burden + ZCD	Isolated current phase reference
Relay interface	ULN2003A + flyback protection	Drives relay coils without loading MCU pins
Capacitor bank	5, 10, 20, 40 μF AC-rated	5 μF resolution; parallel reactive-power compensation
Display	16×2 LCD	Shows PF, bank state, and warnings
Protection	Fuse, isolation, discharge resistors	Limits fault energy and residual capacitor voltage

5. Control Algorithm and Switching Logic

The firmware operates as a closed loop. First, it verifies that both sensing channels are present and that load current exceeds a minimum threshold. It then captures several pairs of voltage and current zero-crossing times, removes the calibration offset, calculates the mean phase angle, and obtains PF. If PF is within the acceptable band, the existing capacitor state is retained. If PF is below 0.95 and the load is lagging, the controller estimates the compensation requirement and searches the available capacitor combinations for the value closest to the calculated requirement. If PF becomes excessively leading or exceeds the upper band, capacitance is removed one step at a time. This cautious stepwise removal prevents abrupt state changes.

To avoid relay chatter caused by noise or small load fluctuations, two stabilization measures are

included. First, the decision uses hysteresis: correction is requested below 0.95, while removal is permitted only after the upper boundary is exceeded or a leading condition is detected. Second, a 2–3 s minimum dwell time is imposed after each switching operation before another decision can be executed. The timer-based phase method is inherited from the low-cost APFC literature [1], [3], and [6], while the use of a decision layer separating measurement from actuation follows the broader digital-control principles evident in [7] and [9].

6. Firmware Procedure

The software sequence is: initialize I/O, timer, LCD, and relay outputs; perform a self-test with all capacitor relays open; acquire voltage and current crossings; reject invalid or missing pulses; calculate Δt , φ , and PF; determine whether the load is lagging or leading from the relative crossing order; calculate the required Q_c and C when correction is needed; map C to the

closest safe capacitor combination; switch relays only at the end of the dwell interval; wait for the circuit to settle; re-measure PF; display PF and bank status; and repeat continuously. A watchdog or timeout returns the system to all-capacitors-off if the measurement sequence becomes invalid. This fail-safe state prevents the controller from leaving an inappropriate capacitor combination connected when the sensing path fails.

7. Prototype Development Procedure

Development is divided into five practical stages. In Stage 1, the sensing circuits are tested at low voltage and adjusted so that their logic transitions correspond to the same physical reference point. In Stage 2, the PIC timing code is verified using two known logic waveforms with controlled delay. In Stage 3, relay outputs are tested with no mains connection to confirm the switching table. In Stage 4, the isolated sensing front end and capacitor bank are integrated with a protected low-power inductive load. In Stage 5, the complete controller is calibrated against a reference power meter. The system should not be judged only by the displayed PF; current reduction, absence of leading over-compensation, repeatability, and stable switching are also recorded.

8. Safety and Calibration Controls

Because the prototype interfaces with mains voltage, the sensing transformers provide galvanic isolation between the high-voltage circuit and the microcontroller. The capacitor branches should include correctly rated AC

capacitors, branch protection, and discharge resistors, and the enclosure should prevent accidental contact with live terminals. Relay contacts must be rated for capacitor inrush current rather than only steady-state current. For calibration, a resistive load establishes the zero-phase reference, a reference meter is used at several inductive operating points, and the measured PF error is recorded before enabling automatic correction. The design is suitable for controlled laboratory development; it should not be connected directly to high-power industrial installations without professional protection engineering and appropriately rated contactors.

9. Evaluation Plan

The evaluation uses five representative inductive load cases at 230 V and 50 Hz. For each case, the initial PF is established, the required capacitance for a 0.95 target is calculated, the nearest available 5 μ F capacitor combination is selected, and the final PF and line current are computed. The line current for a single-phase load is estimated as $I = P/(V \cdot PF)$. The relative current reduction is then calculated from $(I_{\text{before}} - I_{\text{after}})/I_{\text{before}} \times 100\%$. Since this is a methodology paper and no independent field data were supplied, the following results are analytical design-verification values; they demonstrate the expected behavior of the selected capacitor resolution rather than claiming completed industrial measurements.

Results

Analytical Design Verification

Table 3. Analytical verification of the proposed 5/10/20/40 μ F stepped capacitor bank at 230 V, 50 Hz.

Case	Active power (W)	Initial PF	Required C (μ F)	Selected C (μ F)	Final PF	Line current reduction
A	150	0.62	8.46	10	0.988	37.2%
B	300	0.68	13.53	15	0.971	30.0%
C	450	0.74	15.71	15	0.942	21.5%
D	600	0.81	14.27	15	0.956	15.2%
E	750	0.72	28.66	30	0.958	24.8%

The calculations show that the selected capacitor resolution can move a broad range of lagging loads toward the desired operating region. Cases B, D, and E reach approximately 0.96–0.97. Case A is corrected to about 0.988 because the nearest available step is slightly larger than the calculated requirement, while Case C reaches about 0.942 because the 15 μ F selection is slightly smaller than the 15.71 μ F ideal requirement. This result is important: a discrete APFC panel should not be expected to produce exactly the same PF for every load. Its

performance is governed by the capacitor step size, voltage, load magnitude, and target band.

The expected line-current reduction is also significant. At constant active power, raising PF reduces the current required from the source. In the representative cases the calculated current reduction ranges from approximately 15.2% to 37.2%. Because conductor copper loss is proportional to I^2R , a reduction in current also reduces resistive loss and voltage drop. However, the actual energy saving at a particular installation depends on feeder resistance, load

profile, operating time, and any utility tariff for reactive demand; the APFC controller itself does not reduce the active power required by the load.

Control Performance Expectations

The zero-crossing method provides a computationally light PF estimate that is well suited to an 8-bit microcontroller. The primary performance constraints are sensor phase error, timer resolution, and waveform distortion. For nearly sinusoidal inductive loads, averaging several crossings and calibrating the sensing channels should yield stable control. The approach is aligned with the practical timing methods reported by Goyal et al. [1] and Ishak et al. [3]. When distorted current waveforms are present, the measured displacement PF may differ from true PF, so a more advanced rms/real-power measurement method would be needed for highly nonlinear loads.

The switching strategy improves operational stability compared with a simple one-threshold controller. A correction threshold, upper release boundary, and dwell time reduce repeated relay operation when PF fluctuates close to the set point. This is especially important because mechanical relay life is determined by the number and severity of switching operations. The methodology therefore favors slightly slower but stable correction for workshop and laboratory loads instead of continuous high-frequency switching. Intelligent approaches such as those of Sagioglu et al. [8] and Bayindir et al. [5] may provide faster adaptation for complex variable systems, but the deterministic stepped approach offers easier verification and lower implementation complexity.

Comparison with Earlier APFC Approaches

The expected PF range is consistent with the central conclusion of earlier microcontroller APFC studies: timing-based sensing and switched capacitors can move lagging loads closer to unity [1], [2], [4], [6]. The present design differs mainly in its explicit use of a 5 μF resolution bank, two-sided control band, fail-safe all-off state, and disclosure that the table contains analytical verification rather than unreported experimental measurements. This distinction is important for reproducibility. A future hardware paper can use the same test matrix, replace calculated values with measured data, report error against a calibrated power analyzer, and quantify relay response and switching transients.

Conclusion and Discussion

This paper has presented a complete methodology for the design and development of

a microcontroller-based automatic power factor correction system using technology and literature available up to 2017. The proposed architecture uses isolated voltage and current sensing, zero-crossing detection, a PIC16F877A controller, a relay driver, a stepped 5/10/20/40 μF shunt-capacitor bank, and a local display. The controller measures the phase displacement between voltage and current, calculates displacement PF, estimates the required reactive-power compensation, selects a safe capacitor combination, and verifies the result after a stabilization delay. This arrangement follows the practical direction established by PIC- and Arduino-based correction studies [1]–[4], [6] while retaining a simpler deterministic structure than neural or converter-based alternatives [5], [8], [9]. The analytical verification demonstrates the design logic without presenting invented field measurements. For representative 230 V, 50 Hz inductive loads, initial PF values of 0.62–0.81 were improved to approximately 0.94–0.99 using the available capacitor steps. The corresponding calculated source-current reduction was approximately 15–37%. These results illustrate two practical design facts. First, capacitor-bank resolution determines how closely a controller can approach its target. Second, correction should be treated as a bounded control problem rather than an attempt to force PF to exactly 1.0 under every condition. An upper boundary is required because excessive capacitance can produce leading PF and undesirable voltage behavior. From an implementation perspective, measurement quality is as important as the control algorithm. CT and PT channels introduce delays; zero-crossing comparators can be affected by noise; timer quantization becomes significant near unity PF; and distorted load current can make displacement PF an incomplete description of true power quality. The proposed calibration procedure and multi-cycle averaging reduce these errors for conventional inductive loads. For nonlinear electronic loads, future designs should calculate real power from sampled instantaneous voltage and current and should consider harmonic distortion in addition to phase displacement. Solid-state switching may also replace mechanical relays where faster operation or a very high switching count is required. Overall, the proposed methodology is appropriate for a low-cost educational prototype and provides a clear path from requirements to component selection, firmware, safety controls, and validation. Its main contribution is methodological clarity: each calculation and control decision can be reproduced, tested separately, and compared with a reference instrument. Future experimental work should

build the protected prototype, calibrate it against a traceable power analyzer, test resistive-inductive load combinations across the full capacitor range, quantify PF error and switching time, and document thermal and transient behavior. Such testing would convert the present design-verification study into a complete experimental APFC implementation.

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