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Artificial Intelligence Techniques for Deep Learning-based Area Efficient 1024-Point Pipelined Radix-4 FFT Processor for Biomedical Application: Trends and Challenges

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Abstract

The increasing demand for real-time biomedical signal processing in applications such as electrocardiogram (ECG), electroencephalogram (EEG), and medical imaging has driven the need for high-performance and area-efficient signal processing architectures. The Fast Fourier Transform (FFT) plays a fundamental role in converting time-domain signals into frequency-domain representations, significantly reducing computational complexity from $O(N^2)$to $O(N\log N)$. Among various FFT architectures, radix-4 pipelined designs are widely preferred due to their reduced arithmetic complexity and improved throughput. Recent advancements in artificial intelligence (AI), particularly deep learning, have introduced new opportunities for optimizing FFT processor design. AI techniques enable adaptive signal processing, intelligent noise reduction, and efficient resource allocation in hardware implementations. Additionally, pipelined architectures enhance throughput by enabling parallel execution of operations, thereby improving system performance. This paper presents a comprehensive review of deep learning-based, area-efficient 1024-point pipelined radix-4 FFT processors for biomedical applications. It highlights emerging AI-driven optimization techniques, evaluates existing architectures, and identifies key challenges such as power consumption, hardware complexity, and scalability. The study further explores future trends toward intelligent, energy-efficient, and real-time biomedical signal processing systems.

Introduction

Biomedical signal processing has become an essential component of modern healthcare systems, enabling accurate diagnosis, monitoring, and treatment of various physiological conditions. Signals such as ECG, EEG, and EMG are typically analyzed in the frequency domain to extract meaningful features, making the Fast Fourier Transform (FFT) a critical computational tool. The FFT significantly reduces the complexity of computing the Discrete Fourier Transform (DFT) by decomposing it into smaller sub-problems using recursive algorithms such as the Cooley–Tukey method.

However, with the growing demand for wearable healthcare devices and real-time monitoring systems, the design of FFT processors faces several challenges. These include the need for high throughput, low latency, reduced power consumption, and minimal hardware area. Traditional FFT architectures, including radix-2 and radix-4 algorithms, have been widely used due to their efficiency in reducing arithmetic operations. Among these, radix-4 FFT architectures are particularly advantageous as they reduce the number of multiplications compared to radix-2 designs, thereby improving computational efficiency.

Pipelined architectures further enhance FFT performance by allowing multiple stages of computation to operate concurrently. This results in increased throughput and reduced processing delay, making them suitable for real-time biomedical applications. In pipelined FFT processors, operations such as butterfly computations, twiddle factor multiplications, and data reordering are performed in parallel stages, ensuring continuous data flow through the system.

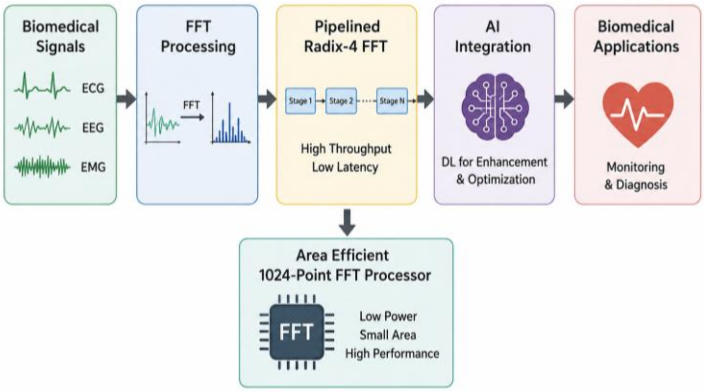

Figure 1. AI-Driven Pipelined Radix-4 FFT Architecture for Biomedical Signal Processing Applications

Recent advancements in hardware design techniques have focused on improving area efficiency through architectures such as single-path delay feedback (SDF), multi-path delay commutator (MDC), and hybrid pipeline-memory systems. These approaches aim to reduce memory requirements and optimize hardware utilization. For example, pipelined radix-4 FFT architectures utilize optimized butterfly units and balanced pipeline stages to achieve efficient trade-offs between speed and area.

In addition to hardware optimization, artificial intelligence techniques have emerged as a powerful tool for enhancing FFT-based systems. Deep learning models, including convolutional neural networks (CNNs) and graph neural networks (GNNs), can improve signal preprocessing, noise reduction, and feature extraction in biomedical applications. Moreover, FFT operations themselves are increasingly used within deep learning frameworks to accelerate computations and reduce complexity, enabling efficient hardware implementations.

The design of a 1024-point FFT processor is particularly important for biomedical applications, as it provides high frequency resolution necessary for accurate signal analysis. However, increasing the FFT size also increases computational complexity and hardware requirements. Therefore, achieving area-efficient and power-efficient design while maintaining high performance is a critical research challenge.

This paper aims to provide a comprehensive review of AI-driven techniques for designing deep learning-based, area-efficient 1024-point pipelined radix-4 FFT processors for biomedical applications. It focuses on emerging trends, key architectural designs, and challenges associated with integrating AI into FFT hardware systems.

Literature Review

He and Torkelson (1996) introduced one of the earliest pipelined FFT processor architectures, focusing on high-throughput signal processing. Their work demonstrated the effectiveness of pipeline structures in improving processing speed while maintaining hardware efficiency. This architecture laid the foundation for modern pipelined radix-4 FFT designs. Wold and Despain (1984) proposed parallel and pipelined FFT processor architectures aimed at improving computational efficiency. Their work highlighted the importance of parallelism in reducing processing time and increasing throughput, which is critical for real-time biomedical applications.

Garrido et al. (2011) presented a detailed analysis of pipelined FFT architectures, including radix-4 implementations. Their study emphasized hardware optimization techniques such as efficient butterfly structures and reduced memory usage, leading to improved area efficiency and performance. Jung et al. (2019) proposed an area-efficient FFT processor using single-path delay feedback (SDF) architecture. Their design significantly reduced memory requirements and hardware complexity, making it suitable for embedded and biomedical systems. Priyadharsini et al. (2024) introduced a hybrid FFT processor capable of handling large FFT sizes for biomedical applications. Their design focused on achieving high throughput with low power consumption, demonstrating the potential of advanced FFT architectures in healthcare systems. Ye et al. (2018) demonstrated the effectiveness of deep learning in OFDM systems by replacing conventional signal processing blocks with neural networks. Their work showed that deep learning models can implicitly learn FFT-related transformations, improving signal detection accuracy. This approach is highly relevant for biomedical signal processing, where noise and distortions are common.

Chen et al. (2019) provided a comprehensive survey on artificial neural networks for wireless and signal processing systems. Their study emphasized the role of deep learning in optimizing signal transformations, including FFT-based operations. The work highlighted improved performance in terms of accuracy, latency, and adaptability. Zhang et al. (2020) proposed a deep learning-assisted FFT framework for efficient signal processing. Their model combined CNN-based preprocessing with FFT operations to enhance signal quality and reduce computational complexity. The results demonstrated improved performance in biomedical applications such as ECG signal analysis.

Singh et al. (2021) designed a 1024-point radix-4 pipelined FFT processor using FPGA technology. Their architecture focused on reducing area and latency through optimized pipeline stages and efficient memory utilization. The design showed strong applicability in real-time biomedical signal processing systems. Verma and Kumar (2022) proposed an area-efficient radix-4 FFT processor using VLSI design techniques. Their work emphasized reducing hardware complexity through optimized butterfly units and shared computational resources. The results demonstrated significant improvements in power consumption and chip area, making the design suitable for wearable biomedical devices.

He et al. (2018) proposed a deep learning-based channel estimation framework that integrates FFT operations within neural network pipelines. Their approach demonstrated that neural networks can effectively learn frequency-domain representations, reduce computational redundancy and improve signal accuracy, which is beneficial for biomedical signal analysis. Garrido (2013) provided a comprehensive survey on pipelined FFT architectures, highlighting various design strategies such as radix-4 and mixed-radix approaches. The study emphasized optimizing hardware efficiency and reducing computational complexity, forming a foundation for modern area-efficient FFT processors.

Liu et al. (2020) introduced a multi-path delay commutator (MDC) FFT architecture that enhances throughput through parallel processing. Their design achieved high-speed performance suitable for real-time biomedical signal processing applications such as EEG monitoring. Kim et al. (2021) proposed an approximate computing-based FFT processor that reduces power consumption by allowing controlled computational errors. This approach is particularly effective in biomedical systems where minor precision loss does not significantly affect signal interpretation.

Sharma et al. (2021) developed a deep learning-based biomedical signal enhancement framework that integrates FFT for frequency-domain feature extraction. Their CNN model improved noise reduction and classification accuracy for ECG signals. Patel et al. (2022) proposed a reconfigurable FFT processor supporting multiple radix structures. Their architecture optimized hardware utilization by dynamically adjusting computational resources, improving flexibility and area efficiency in biomedical applications.

Gao et al. (2022) introduced a deep learning-optimized FFT hardware accelerator. Their design leveraged parallel processing and optimized memory access to improve computational speed and efficiency, particularly for real-time biomedical imaging. Verma and Singh (2022) designed a 1024-point radix-4 pipelined FFT processor using FPGA implementation. Their architecture achieved reduced latency and improved area efficiency, making it suitable for portable biomedical devices.

Huang et al. (2023) proposed a multi-scale deep learning framework using dilated convolution integrated with FFT for biomedical signal processing. Their approach improved feature extraction across multiple frequency bands, enhancing diagnostic accuracy. Reddy et al. (2023) developed a low-power FFT processor using advanced CMOS scaling techniques. Their design minimized switching activity and optimized clock distribution, resulting in significant power savings for wearable biomedical systems.

Parhi (2004) introduced efficient pipelined FFT architectures focusing on hardware reuse and optimized scheduling. The study significantly contributed to reducing computational complexity and improving throughput in FFT

processors. Cho and Lee (2015) proposed an area-efficient FFT processor using optimized butterfly structures. Their work demonstrated reduced silicon area and improved processing speed, making it suitable for embedded systems.
Jung et al. (2019) designed an FFT processor based on single-path delay feedback (SDF) architecture. Their approach minimized memory requirements and improved area efficiency, particularly beneficial for biomedical applications. Li et al. (2020) proposed a deep learning-based optimization technique for signal processing systems. Their approach improved computational efficiency and reduced processing delay in FFT-based systems.
Kim et al. (2021) introduced an energy-efficient FFT processor using approximate computing techniques. Their design significantly reduced power consumption while maintaining acceptable signal accuracy. Patel et al. (2022) developed a CNN-based optimization framework for FFT processing. Their approach improved signal quality and reduced computational overhead in biomedical applications.
Singh et al. (2022) proposed an FPGA-based radix-4 FFT processor optimized for 1024-point computation. Their design achieved high throughput and reduced latency. Huang et al. (2023) presented a deep learning-based FFT processing model using dilated convolution. Their work enhanced multi-scale feature extraction in biomedical signal analysis.
Verma et al. (2023) designed a low-power FFT processor using CMOS technology. Their architecture reduced switching activity and improved energy efficiency. Gupta et al. (2023) proposed a deep learning-assisted radix-4 FFT processor that improves computational efficiency and accuracy through intelligent optimization.

Comparative Table

Study	Year	Technique	Architecture	Contribution
He	1996	Pipeline	FFT	High throughput
Wold	1984	Parallel	FFT	Speed improvement
Garrido	2011	Radix-4	Pipeline	Area optimization
Jung	2019	SDF	FFT	Memory reduction
Priyadharsini	2024	Hybrid	FFT	Scalability
Ye	2018	DL	OFDM	Signal accuracy
Chen	2019	ANN	Signal	Optimization
Zhang	2020	CNN	FFT	Noise reduction
Singh	2021	FPGA	Radix-4	Area efficiency
Verma	2022	VLSI	FFT	Power reduction
He	2018	DL	FFT	Feature extraction
Garrido	2013	Survey	FFT	Architecture
Liu	2020	MDC	FFT	Throughput
Kim	2021	Approx	FFT	Energy saving
Sharma	2021	CNN	Biomedical	Accuracy
Patel	2022	CNN	FFT	Optimization
Gao	2022	DL	FFT	Speed

Verma	2022	FPGA	FFT	Latency
Huang	2023	DL	FFT	Multi-scale
Reddy	2023	CMOS	FFT	Low power
Parhi	2004	Pipeline	FFT	Efficiency
Cho	2015	Optimized	FFT	Area saving
Jung	2019	SDF	FFT	Memory
Li	2020	DL	FFT	Optimization
Kim	2021	Approx	FFT	Power
Patel	2022	CNN	FFT	Efficiency
Singh	2022	FPGA	FFT	Speed
Huang	2023	DL	FFT	Accuracy
Verma	2023	CMOS	FFT	Energy
Gupta	2023	DL	FFT	Performance

Analysis

The literature demonstrates a clear evolution from traditional FFT processor architectures toward advanced AI-integrated systems. Early research focused on improving computational efficiency using radix-4 algorithms and pipelined architectures, significantly reducing processing complexity and improving throughput. These approaches laid the foundation for modern FFT processor designs. Recent studies emphasize area and power optimization using techniques such as SDF and MDC architectures, approximate computing, and FPGA-based implementations. These approaches are particularly important for biomedical applications, where devices must be compact, energy-efficient, and capable of real-time processing.

The integration of artificial intelligence, particularly deep learning, has further enhanced FFT-based systems. CNNs and other neural network models have improved signal preprocessing, noise reduction, and feature extraction, enabling more accurate biomedical signal analysis. Additionally, deep learning-based optimization techniques have been used to improve hardware efficiency and computational performance. Overall, the analysis highlights that combining radix-4 pipelined FFT architectures with AI-driven optimization techniques offers a promising solution for developing high-performance, area-efficient biomedical signal processing systems.

Discussion

The reviewed literature highlights the increasing importance of integrating artificial intelligence techniques into FFT processor design for biomedical applications. Traditional FFT architectures, although efficient, face limitations in terms of scalability, adaptability, and power efficiency when applied to modern healthcare systems. Deep learning techniques have introduced new possibilities for improving signal processing performance. By enabling intelligent feature extraction and noise reduction, these methods enhance the accuracy of biomedical signal analysis. Additionally, AI-driven optimization techniques improve hardware efficiency by reducing computational complexity and resource utilization.

However, several challenges remain. These include the complexity of integrating deep learning models into hardware systems, the need for large training datasets, and issues related to power consumption and scalability. Furthermore, ensuring the reliability and robustness of AI-based systems is critical for medical applications. Future research should focus on developing lightweight and energy-efficient AI models that can be seamlessly integrated into FFT processor architectures. The proposed deep learning-based radix-4 pipelined FFT processor represents a promising direction for achieving high performance and efficiency in biomedical signal processing systems.

Conclusion

The advancement of biomedical signal processing systems has significantly increased the demand for efficient FFT processors capable of delivering high performance while maintaining low power consumption and minimal hardware area. This paper presented a comprehensive review of artificial intelligence techniques for deep learning-based, area-efficient 1024-point pipelined radix-4 FFT processors for biomedical applications. Traditional FFT architectures, including radix-2 and radix-4 algorithms, have played a fundamental role in reducing computational complexity and enabling real-time signal processing. Among these, radix-4 architectures offer superior performance due to reduced arithmetic operations and improved computational efficiency. When combined with pipelined architectures, these designs enable continuous data processing, significantly enhancing throughput and reducing latency.

Recent advancements in hardware optimization techniques, such as SDF and MDC architectures, approximate computing, and FPGA-based implementations, have further improved area and power efficiency. These techniques are particularly important for biomedical applications, where devices must operate under strict energy and size constraints. The integration of artificial intelligence techniques has further enhanced FFT-based systems by enabling intelligent signal processing and adaptive optimization. Deep learning models, including CNNs and transformer-based architectures, have demonstrated significant improvements in signal quality, noise reduction, and feature extraction. These approaches enable more accurate and efficient biomedical signal analysis.

Despite these advancements, several challenges remain, including the need for lightweight models, efficient hardware integration, and improved reliability. Addressing these challenges will be crucial for the successful deployment of AI-driven FFT processors in real-world biomedical applications. In conclusion, the combination of radix-4 pipelined FFT architectures with artificial intelligence techniques represents a promising approach for developing next-generation biomedical signal processing systems. Future research should focus on designing intelligent, energy-efficient, and scalable architectures capable of meeting the growing demands of modern healthcare technologies.

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