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### From Transistors to Quantum Dots: A Comparative Study of CMOS and QCA Paradigms Technologies

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Email: <sup>1</sup>vrushali.nasre@pcenagpur.edu.in, <sup>2</sup>amgaonkarshubhroto@gmail.com, <sup>3</sup>rohititware03@gmail.com, <sup>4</sup>harshalvaidya0506@gmail.com, <sup>5</sup>priyanshubhagat29@gmail.com

Peer Review Information	Abstract
<p><i>Submission: 05 Nov 2025</i></p> <p><i>Revision: 25 Nov 2025</i></p> <p><i>Acceptance: 17 Dec 2025</i></p> <p><b>Keywords</b></p> <p><i>Quantum-dot Cellular Automata, CMOS, QCA designer tool, Nanotechnology, Semiconductor, integrated Circuit Design, Logic Gates.</i></p>	<p>(CMOS) Complementary-Metal-Oxide Semiconductor technology has been the dominant platform for digital circuit design for decades, enabling high-performance and cost-effective electronics. However, as CMOS devices scale below 5 nm, they face physical and economic challenges such as leakage currents, short-channel effects, and increased fabrication costs. Quantum-dot Cellular Automata (QCA) is an emerging nanotechnology that encodes binary information using electron polarization rather than current flow, offering ultra-low power consumption and extremely high device density. This paper presents a comparative review of CMOS and QCA technologies in terms of power, area, speed, scalability, reliability, and fabrication complexity. Challenges and future trends for both technologies are also discussed, providing an overview of their possible roles in next-generation Nanoelectronics. The paper also discusses current challenges and potential research directions for enabling a transition from CMOS to QCA in the coming decades.</p>

#### Introduction

##### 1. CMOS Technology Overview:

CMOS technology was built in 1963 by Frank Wanlass while working at Fairchild Semiconductor. CMOS is a combination of N-type and P-type MOSFET (Metal Oxide Semiconductor Field Effect Transistor). CMOS technology is used to build integrated circuits, microprocessors, microcontrollers, detectors, RAM (Random Access Memory) and many other digital circuits. Gordons Moore observed that the number of transistors in an integrated circuit doubles every 18 months [1]. This world of computerized electronics demands more and more biases. This can be achieved by spanning CMOS technology from millimeters to many nanometers in instantaneous technologies [2].

In recent years, non-flat technology by

industries. This facilitates the manufacturing of high-speed integrated circuits, processors and other electronic devices. Scientists are making a very sharp reduction in CMOS size to 7 nm in future CMOS technologies [3]. The use of graphene is preferred in the future and currently in 3D (three-dimensional) technology. The latest material used for CMOS design is graphene [4]. Graphene has very attractive properties: high electron and hole mobility, planar structure, high thermal conductance, high current carrying capacity and thin body [5]. New technology innovations are very important to reduce the size of CMOS integrated circuits [6]. After Bipolar Junction Transistor MOSFET (Metal Oxide Semiconductor Field Effect Transistor) comes with very interesting features like: low power consumption, low operating voltage,

higher speed, etc., which make MOSFET useful in electronic design. Two types of MOS transistors, PMOS and NMOS, are invented and used to design integrated circuits. Both types have very high static power consumption. This problem is solved if and only a logic designed in such a way that it does not consume power in static state. After decades, Frank Wanlass introduces a new logic designed using two complementary p- and n-type MOSFETs. Two main advantages of CMOS technology are high noise immunity and very low static power consumption [7].

In recent decades there have been innovations in new CMOS technologies with excellent characteristics. MOS IC Size Reduction Trends

(1970) (2D technology)  $10\mu\text{m} \rightarrow 8\mu\text{m} \rightarrow 6\mu\text{m} \rightarrow 4\mu\text{m} \rightarrow 3\mu\text{m} \rightarrow 2\mu\text{m} \rightarrow 1.2\mu\text{m} \rightarrow 0.8\mu\text{m} \rightarrow 0.5\mu\text{m} \rightarrow 0.35\mu\text{m} \rightarrow 0.25\mu\text{m} \rightarrow 180\text{nm} \rightarrow 130\text{nm} \rightarrow 90\text{nm} \rightarrow 65\text{nm} \rightarrow 45\text{nm}$  (2005)  $\rightarrow 32\text{nm}$  (2007)  $\rightarrow 28\text{nm}$  (2009)  $\rightarrow 22\text{nm}$  (2012) (3D technology)  $\rightarrow 15\text{nm}$  (2013)  $\rightarrow 10\text{nm}$  (2015)  $\rightarrow 7\text{nm}$  (2017)

*Fig.1. Trend of downsizing for MOS, HCMOS integrated circuits [3-6].*

## 2. QCA Technology Overview:

Since the 1970s, the device used for higher levels of integration has been the field effect transistor (FET). Transistor size is reduced by about half every 18 to 24 months, as Moore predicted. The International Technology Roadmap for Semiconductors (ITRS) says that scaling of current FET-based ICs will reach manufacturing limits by 2020. Beyond further reduction of physical and power density limitations, scaling of ICs in contemporary complementary metal-oxide semiconductor (CMOS) manufacturing technology would be further prohibited. To continue expanding electronic devices, microelectronics industries must move from the conventional FET-based paradigm to an alternative paradigm of information representation and processing. This paradigm shift should also encompass the tools and design cultures that have made today's CMOS technology possible. The manufacturing of quantum dots using new technologies offers an alternative to CMOS technology. The binary information is encoded in terms of the charge of the quantum dot cells and is called quantum dot cellular automata (QCA), which basically computes using quantum dots [8]. The first computer was designed using electromechanical switches and relays. These switches were later replaced by vacuum tube triodes. Over time, transistors replaced these triodes. CMOS technology, which involves designing circuits using MOSFETs, has several advantages such as

area occupation, power dissipation, switching speed, etc. According to Moore's law, the number of devices manufactured on a substrate doubles every 18 months. But with the ongoing changes and inventions in the semiconductor industry. CMOS technology has almost reached saturation. Therefore, other technologies are being investigated for this purpose. This article mainly focuses on a survey and study of various research domains for Beyond CMOS i.e. other similar technologies in Section 2. In Section 3 we discuss the taxonomy of various topics related to QCA and in Section 4 the basic terminologies and concepts involved with QCA. This section describes basic gates and other logic structures. Section 5 provides examples of simulation results. The last section describes the future scope in the design using QCA along with the conclusion [9].

S. et al. in their paper [18] presents a novel model for the logic synthesis of quantum dot cellular automata circuits, emphasizing energy dissipation, a crucial aspect in the energy efficiency of QCA technology. The paper [17] by G Cocorullo et.al presents innovative logic strategies and QCA modules specifically designed to improve computational speed without increasing area or cell count. Showing the potential for efficient QCA-based implementations of decimal adders [17]. The research paper [19] presents a novel design for a QCA Decimal Full Adder (DFA) circuit, aiming to improve efficiency and performance. Inverters and majority gates are fundamental building blocks in QCA circuits, and the 3-input majority gate is used less efficiently in technology mapping. The research work carried out by Liolis et.al. in paper [19] is a significant contribution to addressing the complex timing challenges in QCA circuits, offering a universal design tool applicable to existing designs without additional complexity. The challenge of feedback design in sequential QCA circuits, particularly in line feedback shift registers (LFSR), is addressed in the paper [20].

### 2.1. QCA Cells and Wire

A QCA circuit is made up of QCA cells; The arrangement of the cells determines the functions of the circuit. A standard QCA cell consists of four quantum dots, two of which are electrons that can occupy opposite diagonal positions within the cell. This diagonal location of the electrons represents the binary logic states: logic "1" and logic "0." Figure 1 shows the structure of a QCA cell, illustrating its two configurations representing logic '1' (left) and logic '0' (right). Figure 2 shows a normal and a rotated QCA cable. QCA cables are nothing more

than sequences of QCA cells. In a normal cable, the input signal is transmitted along the cable. On the other hand, a twisted cable can reverse or maintain the signal depending on its configuration and the number of cells. Figure 3 illustrates the signal propagation in normal and rotated QCA cables [10].

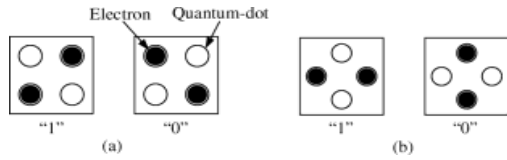


Fig. 2. QCA cells [10]

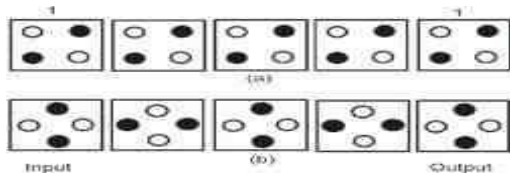


Fig. 3. (a) Normal wire, (b) Rotated wire. [10]

2.2. Majority Gates & Inverter

The majority gate is a basic element in QCA circuits. A 3-way voter majority (MV) is expressed as:

$$M(A, B, C) = AB + BC + CA$$

This gate is capable of implementing logic gates such as AND and OR. For example, a 2-input AND gate can be made by keeping one of its inputs at logic "0" and an OR gate at logic "1." The structure of a majority gate is depicted in Fig.5, while Fig.5 demonstrates the realization of AND and OR gates using majority logic. In addition to majority gates, inverters are essential in QCA-based designs. An inverter inverts the input signal and generates the opposite logic state. Figure 4 illustrates the basic structure of a QCA inverter. These logic elements form the basis for complex circuit designs in QCA [10].

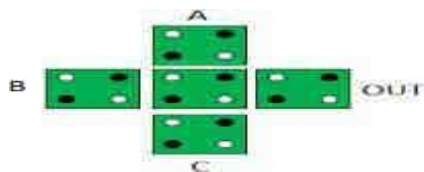


Fig. 4. Structure of the 3-input Majority Voter (MV) [10].



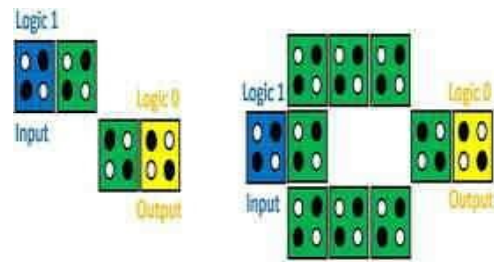
Fig. 5. Realization of AND and OR gates using the Majority Voter (MV) [10].

2.3. QCA Clocking

QCA circuits use a synchronization mechanism to control signal propagation through different zones. There are four phases of timing. During the first phase, the cells' potential barriers are reduced, causing the cells to depolarize. The barriers are then lifted, polarizing the cells and allowing them to perform logical

Fig. 6. Structure of a QCA Inverter [10]

operations. In the next phase, the barriers decrease again, allowing the cells to depolarize. In the Final phase, the barriers remain low,



maintaining the non-polarized state. These phases allow the sequential propagation of signals through different zones, ensuring the synchronized operation of the QCA circuits. Fig.7 shows the timing zones and their phases in QCA [10].

A quantum clock controls the behaviour of quantum dot cells in four stages by affecting their tunnelling barriers.

- In the first phase, the barriers begin to increase.
- The barriers are high enough to prevent electron tunnelling in the second stage.
- In the third step, the barriers begin to become poorer.
- In the next step, the barriers become low, allowing the electrons to tunnel freely. Electrons can move easily when the timing pulse is high; when the synchronization pulse is low, the cell locks its state [11].

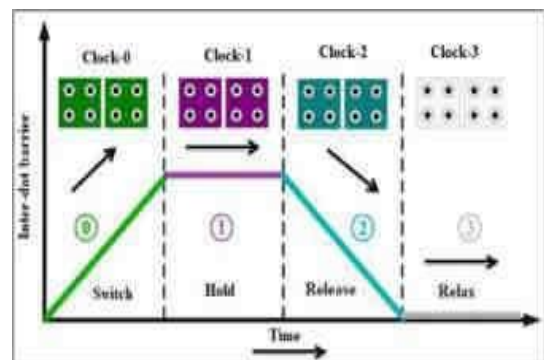


Fig. 7. Clock Phases [10].

#### 2.4. QCA Crossover

In complex QCA circuits, it is often necessary to route signals over each other without interference. This is achieved through QCA crosses. There are two main types of junctions: coplanar and multilayer.

- **Coplanar** crossings use rotated cells to allow signals to pass each other in the same plane without interaction.
- **Multilayer** crossovers, on the other hand, involve routing signals on separate layers to avoid conflicts.

These crossovers play a critical role in ensuring efficient and interference-free signal routing in larger QCA designs [10].

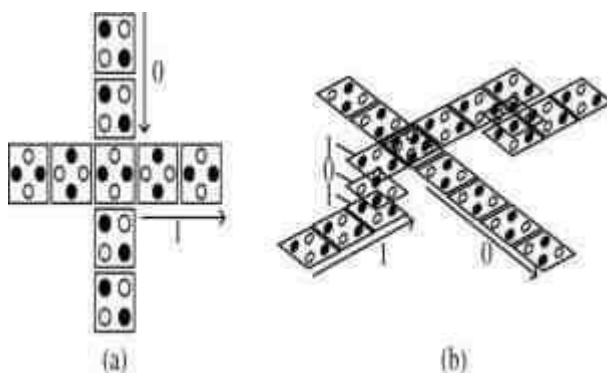


Fig. 8. Types of QCA Crossovers: (a) Coplanar, (b) Multilayer.

#### 2.5. QCA Designer Tool

QCA Designer is a continually evolving tool designed to facilitate fast and accurate simulation and design of QCA circuits, compatible with most standard platforms. QCA Designer is an open QCA circuit design and simulation software. It is industrialized by the Walus Group at the University of British Columbia (CA). This work uses C/C++ and incorporates several open-source software tools, including the GNU Image Manipulation Program Toolkit graphics library. It is governed by the GNU General Public License (GPL) as open-source software. This development approach allows QCA Designer to be compiled and used in various applications. This work aims to create a user-friendly and easily accessible design and simulation tool for the online research community. A key goal of the design is to allow other developers to seamlessly integrate their utilities into QCA Designer, which is achieved by providing a consistent method of representing information within the software [11].

The fundamental steps in designing and simulating a QCA circuit include:

1. QCA circuit layout with QCA cells.

2. Definition of the inputs and outputs of the circuit.
3. Configuration of the circuit's check-in areas.
4. Configure the simulation engine
5. Simulate the QCA circuit and witness the waveforms.
6. Debug the design and rerun the simulation until accurate waveforms are obtained.

Fig. 9 Main interface of QCA Design Tool After installing the QCA Designer software on a Windows operating system, navigate to "Windows -> All Programs -> QCA Designer -> QCA Designer" to launch the application. The main interface of the software will be displayed [11].

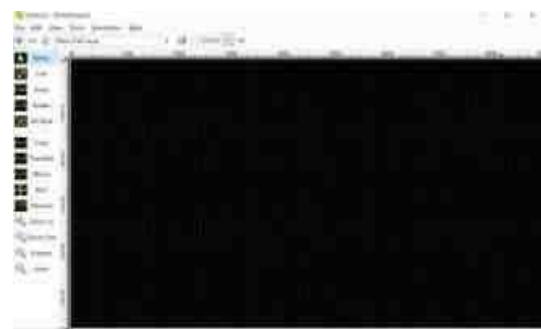


Fig. 9. Main interface of QCA designer tool [11]

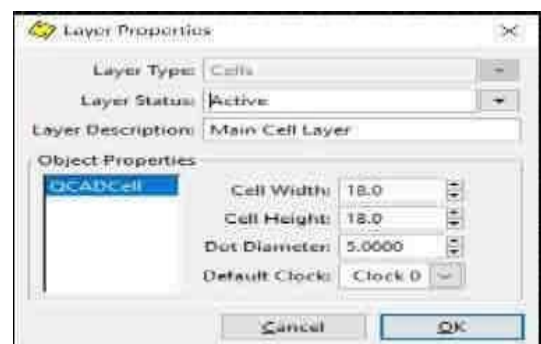


Fig. 10. Setting properties in QCA designer [11]

To view the properties of the current layer, click the "Edit -> Layer Properties" menu. This will display the configuration of the active layer: each QCA cell has a width and height of 18.0  $\mu\text{m}$ , with a 2.0  $\mu\text{m}$  gap between adjacent cells. Therefore, the centre-to-centre distance between adjacent cells is 20  $\mu\text{m}$ . Each quantum dot inside a QCA cell has a diameter of 5  $\mu\text{m}$  and the default clock zone for a QCA cell is set to "Clock 0".

Next, save your design by clicking "File -> Save". A pop-up window will appear asking you to select a directory and name for the layout. The design name must have a "QCA" extension (e.g. exor1.qca, though any name can be used). Click

"OK" to save the design.



Fig. 11. Save option in QCA designer tool [11]

**Proposed Design of Logic Gates in CMOS and QCA**

The basic logic gate designs, shown in Figures 12 to 21, illustrate circuit diagrams implemented with PMOS and NMOS transistors, designed and simulated using LTspice software.

**1. CMOS Technology**

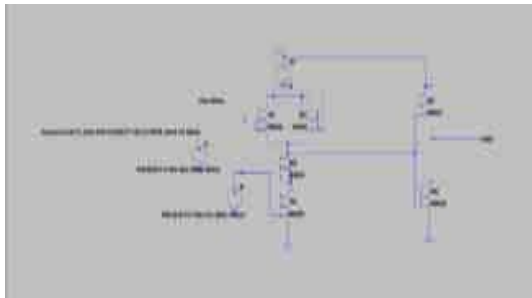


Fig. 12.1. Design of AND Gate Using CMOS-based Technology

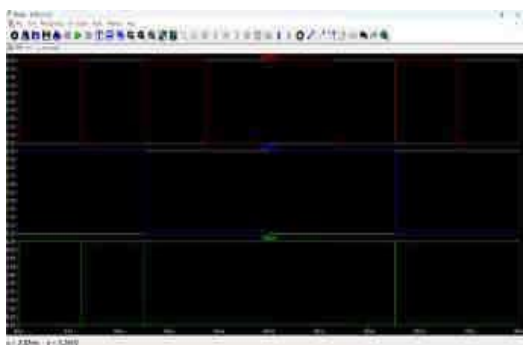


Fig. 12.2. Simulation of AND Gate Using CMOS-based Technology

**CMOS AND Gate Design and Simulation:**

In CMOS technology, an AND gate is constructed using a NAND gate followed by an inverter. The NAND has two PMOS transistors in parallel (pull-up) and two NMOS transistors in series (pull-down), giving an output  $(A \cdot B)'$ , which the inverter converts to  $Y = A \cdot B$ . Simulation using

SPICE/Verilog confirms correct logic behavior with full voltage swing: the output is high only when both inputs are high, and propagation delay and switching can be observed from the transient response.

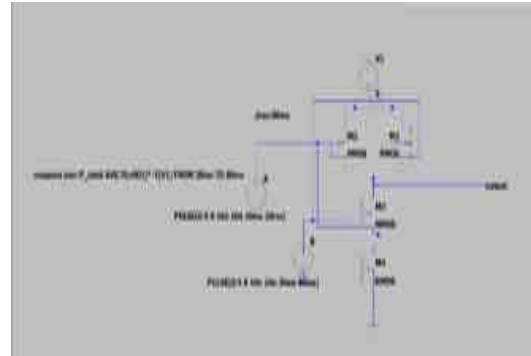


Fig. 13.1. Design of NAND Gate Using CMOS-based Technology

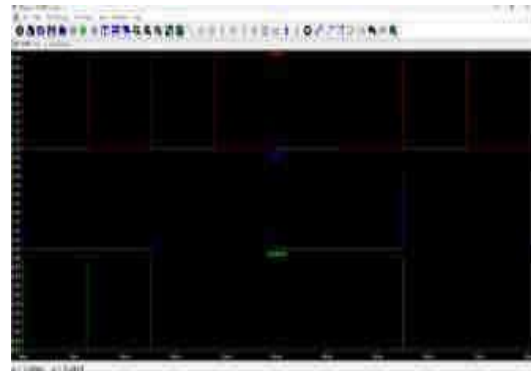


Fig. 13.2. Simulation of NAND Gate Using CMOS-based Technology

**CMOS NAND Gate Design and Simulation:**

In CMOS technology, a NAND gate uses two PMOS transistors in parallel (pull-up) and two NMOS transistors in series (pull-down) to produce  $Y = (A \cdot B)'$ . The design includes inputs A and B with transistor networks, ensuring high noise margin and reliable switching. The simulation confirms the correct logic: the output stays high except when both inputs are high, with rise/fall times and propagation delay observable from transient analysis.

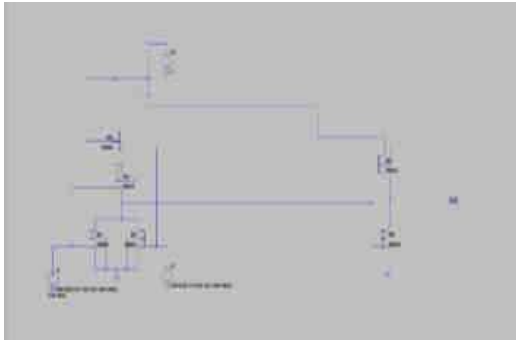


Fig. 14.1. Design of OR Gate Using CMOS-based Technology

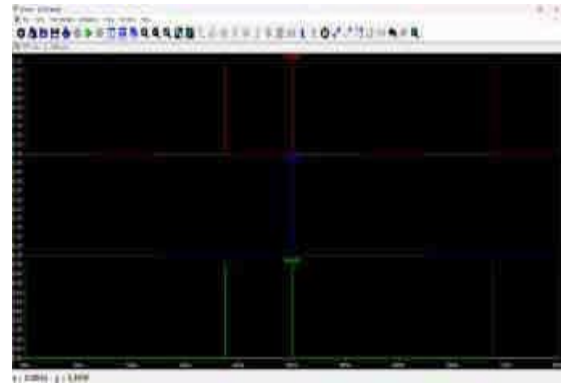


Fig. 15.2. Simulation of NOR Gate Using CMOS-based Technology

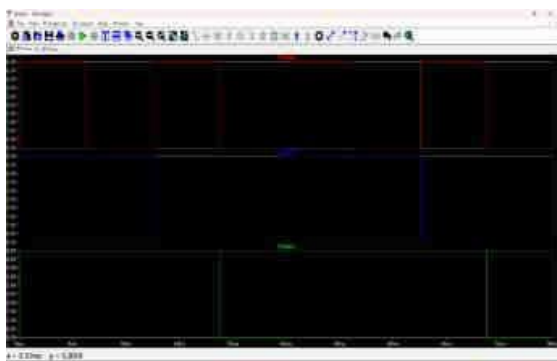


Fig. 14.2. Simulation of OR Gate Using CMOS-based Technology

*CMOS NOR Gate Design and Simulation:*

In CMOS technology, a NOR gate uses two PMOS transistors in series (pull-up) and two NMOS transistors in parallel (pull-down) to produce  $Y=(A+B)'$ . The design includes inputs A and B with transistor networks, ensuring full logic oscillation and robust operation. Simulation with inputs A and B confirms the correct logic: the output is high only when both inputs are low, with appropriate voltage levels and transition times observable from waveform analysis.

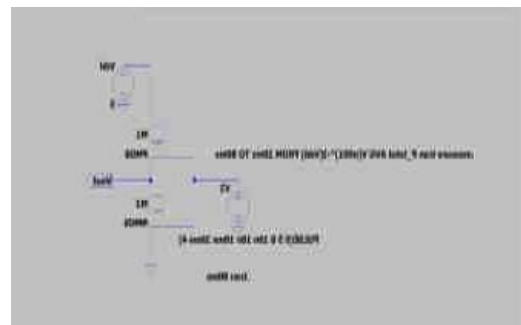


Fig. 16.1. Design of NOT Gate Using CMOS-based Technology

*CMOS OR Gate Design and Simulation:*

In CMOS technology, an OR gate is constructed using an NOR gate followed by an inverter. The NOR gate has two PMOS transistors in series (pull-up) and two NMOS transistors in parallel (pull-down), giving an output  $(A+B)'$ , which the inverter converts to  $Y=A+B$ . Simulation with inputs A and B confirms the correct logic: the output is high when either input is high and low only when both are low, with delay and switching observable from transient analysis.

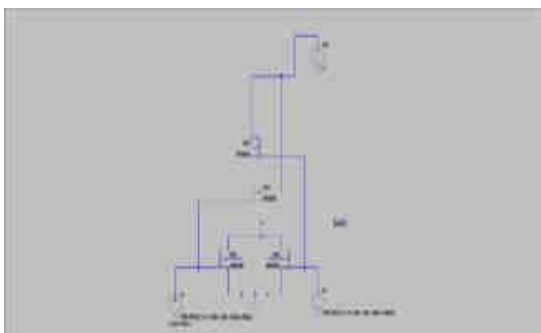


Fig. 15.1. Design of NOR Gate Using CMOS-based Technology



Fig. 16.2. Simulation of NOT Gate Using CMOS-based Technology

*CMOS NOT Gate Design and Simulation:*

In CMOS technology, a NOT (inverter) gate uses a single pair of PMOS and NMOS transistors. The PMOS connects to VDD, NMOS to GND and the input is applied to both gates; the output  $Y=A^{\wedge}$  is taken from their common drain. The design ensures full logic oscillation, fast switching and low static power. The simulation confirms the correct inversion of input A, with total voltage swing and adequate transient response.

2. QCA Technology



Fig. 17.1. Design of AND Gate Using QCA-based Technology

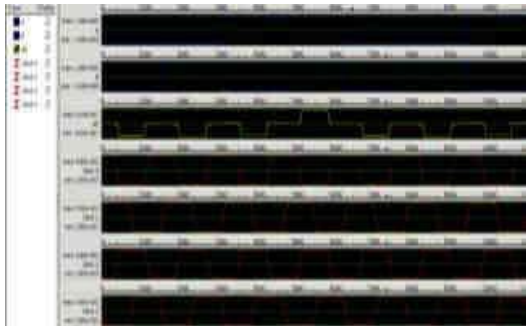


Fig. 17.2. Simulation of AND Gate Using QCA-based Technology

*QCA AND Gate Design and Simulation:*

In quantum-dot cellular automata (QCA), logic circuits are built using majority gates (MGs) and inverters (INVs). Each QCA the cell contains four quantum dots and two mobile electrons, representing binary states by polarization:  $P=+1$  for logic '1' and  $P=-1$  for logic '0'.

The AND gate is implemented using a 3-input majority gate where one input is fixed to logic '0', giving  $AND(A,B) = M(A,B,0) = AB$ . The layout includes input lines for A and B, a fixed logic-0 cell, and an output cell representing  $A \cdot B$ . The

simulation monitors the polarization of all cells using the QCA design tool. The output cell is correctly polarized to '1' only when both inputs are '1', and verify the AND logic function. The design ensures reliable operation with proper signal propagation in the cell network.



Fig. 18.1. Design of NAND Gate Using QCA-based Technology

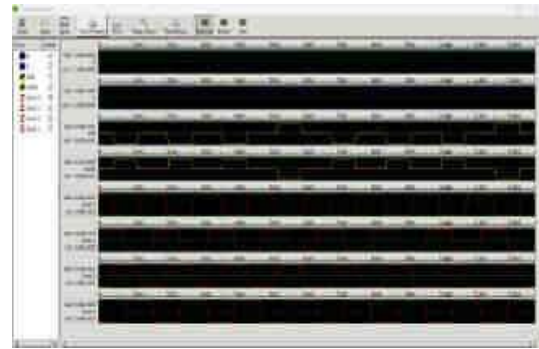


Fig. 18.2. Simulation of NAND Gate Using QCA-based Technology

*QCA NAND Gate Design and Simulation:*

In quantum-dot cellular automata (QCA), logic circuits use majority gates (MGs) and inverters (INVs) as fundamental components. Each QCA cell contains four quantum dots and two mobile electrons, with polarization  $P=+1$  for logic '1' and  $P=-1$  for logic '0'.

The NAND gate is implemented by first creating an AND gate using a 3-input majority gate, with one input fixed to logic '0':  $AND(A,B)=M(A,B,0)=A \cdot B$ . The AND output is then inverted using a QCA inverter to obtain  $NAND(A,B)=(A \cdot B)^{\wedge}$ . The layout includes input lines A and B, fixed logic-0 cells, AND gate regions, and an inverter section for the final output.

The simulation applies inputs A and B, monitors the polarization of all cells, and confirms correct NAND logic: the output is high when both inputs are high. Clocking zones ensure proper sequential propagation, and transient analysis

demonstrates reliable inversion with no metastable states.



Fig. 19.1. Design of OR Gate Using QCA-based Technology

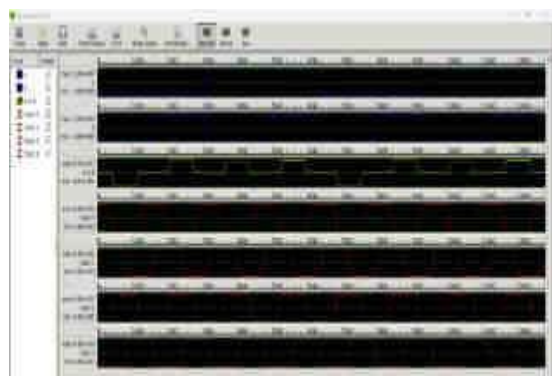


Fig. 19.2. Simulation of OR Gate Using QCA-based Technology

**QCA OR Gate Design and Simulation:**

In quantum dot cellular automata (QCA), logic circuits use majority gates (MG) and inverters (INV). Each QCA cell has four quantum dots and two mobile electrons, with polarization  $P = +1$  for logic '1' and  $P = -1$  for logic '0'.

The OR gate is implemented using a 3-input majority gate with one input set to logic '1':  $OR(A,B) = M(A,B,1) = A+B$ . The layout includes input lines A and B, fixed logic cell 1, and an output cell representing  $A+B$ .

Simulation applies inputs A and B, monitors cell polarization, and confirms correct OR logic: the output polarizes to '1' if either or both inputs are '1', and '0' only when both inputs are '0'. Polarization propagates smoothly through the majority gate, controlled by four QCA clocking phases, with minimal delay observed across cells.

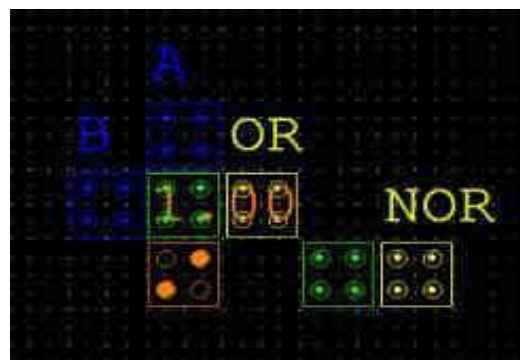


Fig. 20.1. Design of NOR Gate Using QCA-based Technology



Fig. 20.2. Simulation of NOR Gate Using QCA-based Technology

**QCA NOR Gate Design and Simulation:**

In quantum dot cellular automata (QCA), logic circuits use majority gates (MG) and inverters (INV). Each QCA cell has four quantum dots and two mobile electrons, with polarization  $P = +1$  for logic '1' and  $P = -1$  for logic '0'.

The NOR gate is implemented by first forming an OR gate using a 3-input majority gate with one input set to logic '1':  $OR(A,B) = M(A,B,1) = A+B$ . The OR output is then inverted using a QCA inverter to produce  $NOR(A,B) = (A+B)'$ . The layout includes input lines A and B, fixed logic cell, the OR gate region and an inverting section for the final output.

The simulation applies inputs A and B, monitoring the cell polarization. The output is correctly biased to "1" only when both inputs are "0". The four-phase QCA synchronization system ensures synchronous propagation, proper output stabilization in each clock cycle, and no bias conflicts.



Fig. 21.1. Design of NOT Gate Using QCA-based Technology

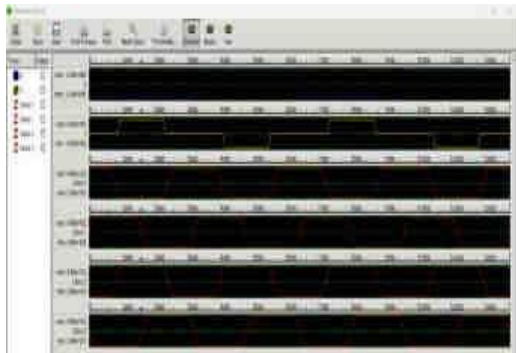


Fig. 21.2. Simulation of NOT Gate Using QCA-based Technology

**QCA NOT Gate Design and Simulation:**

In quantum dot cellular automata (QCA), logic circuits use majority gates (MG) and inverters (INV). Each QCA cell has four quantum dots and two mobile electrons, with polarization  $P = +1$  for logic '1' and  $P = -1$  for logic '0'. The NOT (inverting) gate inverts the input bias:  $Y=A^{\wedge}$ . Its design includes an input cell, cross-coupled QCA cells, and an output cell placed diagonally to induce opposite polarization through electrostatic interaction. The simulation applies input A and monitors the bias of the output. The inverter correctly produces the complementary logic state for both input levels. The four-phase QCA (switch, hold, release, relax) synchronization system ensures smooth, synchronized and stable polarization propagation without failure.

**Comparative Review of CMOS and QCA**

Articles [12-16] are considered to identify the main differences between QCA and CMOS technologies and are presented in Table. I. Table I Comparison between QCA and CMOS technology.

**Table I.** Comparative Review of CMOS and QCA

Parameters	QCA	CMOS
Power consumption [12]	Extremely low	High
Speed [13]	High	Slower
Size and Density [12]	Higher	Lower
Heat dissipation [16]	Low	High
Design complexity [14]	Requires novel design method and tools	Matured design eco system and established tools
Reliability [16]	Susceptible to fabrication defects and quantum effects	More reliable
Manufacturing complexity [13]	Complex due to nanoscale precision required for quantum dots	Advanced but standardized manufacturing techniques
Scalability [16]	Highly scalable	Facing challenges due to physical limits
Operation temp [15]	Requires operation at cryogenic Temperatures.	At room temperature
Commercial viability [14]	Still in research phase, not yet commercially viable	Widely used and commercially viable



## Conclusions

This article presented a comparative analysis of CMOS and Quantum-dot Cellular Automata (QCA) technologies. While CMOS technology has achieved remarkable scaling over decades, it now faces physical and manufacturing limitations. QCA emerges as a potential successor, offering ultra-low power consumption, high speed, and nanoscale integration capabilities. Basic logic gates and combinational circuits implemented using QCA design tools demonstrate their feasibility for digital computing. However, more research is required to overcome challenges related to manufacturing accuracy, temperature stability, and large-scale integration. With continued advancements, QCA technology could become a viable alternative for future quantum computing and nanoelectronics applications. Study highlights QCA's potential to revolutionize digital circuits, paving the way to more efficient and powerful computing systems

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