



Comparative Study of PWM Techniques for Three-Phase Inverter Systems

Saffiya Wannenmacher

Department of Electrical and Computer Engineering, Tonle Sap Institute of Engineering and Commerce, Cambodia

saffiya.wannenmacher@tsiec-kh.org

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Abstract

Pulse-width modulation (PWM) is the central control mechanism used to synthesize adjustable three-phase AC voltages from a fixed DC link in voltage-source inverters. The choice of PWM strategy directly affects harmonic distortion, DC-bus utilization, switching activity, acoustic behavior, and implementation complexity. This paper presents a controlled methodology for comparing four representative PWM techniques for a two-level three-phase inverter: sinusoidal PWM (SPWM), third-harmonic-injection PWM (THIPWM), carrier-equivalent space-vector PWM (SVPWM), and a discontinuous upper-clamping PWM (DPWM) variant. All methods are evaluated under identical electrical conditions: a 400 V DC link, 50 Hz fundamental frequency, 5 kHz carrier frequency, modulation index of 0.9, and a balanced 10 Ω -20 mH star-connected load. Performance indicators include line-to-line fundamental RMS voltage, phase-current fundamental RMS value, phase-current total harmonic distortion (THD), maximum linear DC-bus utilization, and switching transitions per phase leg. The numerical comparison indicates that SVPWM provides the lowest simulated current THD (0.81%) at the common operating point, THIPWM closely follows (0.84%), while SPWM gives 0.93%. The representative DPWM case reduces gate transitions from approximately 200 to 133 per phase leg per fundamental cycle, at the cost of moderately higher current THD (1.12%). The study confirms that there is no universally superior PWM method; the preferred technique depends on whether waveform quality, voltage utilization, switching loss, or algorithmic simplicity is dominant.

Introduction

Three-phase voltage-source inverters (VSIs) are widely used in variable-speed motor drives, renewable-energy interfaces, uninterruptible power supplies, active filters, and grid-connected power conversion. A two-level VSI can only connect each phase terminal to one of two DC-link potentials; therefore, a PWM algorithm is required to arrange high-frequency switching states so that the average phase and line voltages follow a low-frequency reference. The quality of

this synthesis determines the harmonic current in the load, the available fundamental output voltage, semiconductor switching losses, and the computational burden placed on the digital controller.

The classical sinusoidal carrier method remains attractive because it is intuitive and easily implemented using a comparison between sinusoidal references and a triangular carrier. However, space-vector formulations demonstrated that a three-phase inverter can

exploit the available switching states more effectively. Van der Broeck, Skudelny, and Stanke (1988) showed that voltage-space-vector modulation can reduce current harmonics and increase the attainable modulation range compared with conventional sinusoidal PWM. Holmes (1992) subsequently established a mathematical relationship between regular-sampled carrier PWM and space-vector modulation, reinforcing the idea that many apparently different PWM families are alternative realizations of common volt-second principles.

The present study is therefore designed as a controlled methodology paper rather than a survey alone. Its objective is to compare commonly used PWM strategies under identical inverter, carrier, load, and modulation conditions. The specific research questions are: (i) how do SPWM, THIPWM, SVPWM, and a discontinuous clamped PWM variant differ in current harmonic performance; (ii) which continuous methods make better use of the available DC link; and (iii) what switching-activity reduction can be obtained through discontinuous clamping? The analysis is intentionally limited to concepts and references available up to 2016.

Literature Review

PWM research for three-phase inverters has evolved from carrier-intersection approaches toward unified carrier-based and space-vector interpretations. Van der Broeck et al. (1988) provided an early analytical and experimental comparison of sinusoidal modulation and voltage-space-vector modulation. Their work established two enduring advantages associated with space-vector synthesis: reduced current harmonic content and a higher usable modulation index. Holmes (1992) then showed that regular-sampled PWM and space-vector modulation are mathematically related when the switching sequence and zero-sequence components are properly interpreted. These studies form the theoretical basis for comparing SPWM with zero-sequence-injected methods.

A second research direction focused on the trade-off between waveform quality and switching losses. Hava, Kerkman, and Lipo (1998) developed a generalized discontinuous PWM framework in which one phase can be clamped for portions of the fundamental period, reducing switching effort while retaining controllable output voltage. Their later analytical treatment of carrier-based PWM-VSI drives provided

comparative tools for current ripple, switching losses, and voltage linearity, enabling PWM strategies to be evaluated using common performance measures (Hava et al., 1999). These results are directly relevant to the present inclusion of a representative discontinuous clamping method.

The relationship between carrier-based PWM and space-vector PWM was further clarified by Zhou and Wang (2002), who systematically related modulation signals, zero-sequence injection, switching patterns, vector sectors, and zero-vector distribution. Their analysis is particularly important for a fair comparison because an SVPWM waveform can be implemented through carrier comparison after adding an appropriate common-mode offset. For multilevel systems, Wang (2002) similarly demonstrated that sine-triangle and space-vector modulation can be made equivalent through suitable common-mode injection or redundant-state dwell-time selection. McGrath, Holmes, and Lipo (2003) extended this equivalence to optimized space-vector switching sequences and demonstrated that properly centered sequences give favorable harmonic characteristics.

Later comparative work reinforced the importance of implementation details rather than simply naming the modulation family. Yao, Hu, and Lu (2008) compared space-vector and carrier-based modulation and showed that the additional freedom in switching-state selection can be exploited to optimize voltage quality and other converter objectives. Finally, Binoj Kumar, Saritha, and Narayanan (2016) experimentally compared conventional and bus-clamping PWM methods in induction-motor drives and emphasized the trade-off between switching loss and harmonic or acoustic behavior. Collectively, the literature supports a multi-criterion comparison using waveform quality, voltage utilization, and switching activity rather than THD alone.

Methodology

1. Research Design and Common Inverter Model

A numerical switching model of a two-level, three-phase VSI is used. Each inverter leg contains complementary upper and lower devices. Ideal switches are assumed for the core PWM comparison so that differences arise from the modulation strategy rather than unequal device models. The DC link is fixed at 400 V. A balanced three-wire, star-connected RL load is used with $R = 10 \, \Omega$ and $L = 20 \, \text{mH}$ per phase. The

fundamental reference frequency is 50 Hz, and the triangular carrier frequency is 5 kHz, giving a frequency ratio of 100. The common fundamental modulation command is $m = 0.9$, which keeps every method within its linear operating region. A numerical time step of $2 \mu\text{s}$ is used, corresponding to a 500 kHz simulation sampling rate.

2. PWM Algorithms

SPWM: Three sinusoidal references displaced by 120° are compared directly with the same symmetrical triangular carrier. For phase a, the normalized reference is $v_a^* = m \sin(\omega t)$, with equivalent expressions for phases b and c. SPWM is treated as the baseline because it requires minimal computation and provides fixed-frequency switching.

THIPWM: A zero-sequence third-harmonic term is added equally to all three sinusoidal phase references: $v_z = (m/6) \sin(3\omega t)$. Because the same zero-sequence component appears in all phases, it cancels from the line-to-line fundamental voltage. The flattened reference peaks allow a larger fundamental reference before the carrier limit is reached. This principle

is consistent with the carrier/space-vector relationships discussed by Zhou and Wang (2002).

SVPWM: A carrier-equivalent SVPWM implementation is used. At each time step, the maximum and minimum of the three sinusoidal references are identified and a common offset $v_0 = -0.5(v_{\max} + v_{\min})$ is added to all three phase commands. This zero-sequence injection centers the reference set within the carrier boundaries and reproduces the centered space-vector switching behavior discussed in the literature (Holmes, 1992; McGrath et al., 2003).

DPWM: A representative upper-clamping discontinuous method is included to expose the switching-loss trade-off. A common offset $v_0 = 1 - v_{\max}$ is added so that the phase with the largest instantaneous reference is clamped to the positive carrier boundary. The method is not intended to represent every generalized DPWM angle; rather, it provides a reproducible discontinuous clamping case consistent with the principle that clamping reduces switching activity (Hava et al., 1998; Binojkumar et al., 2016).

Table 1. Common Simulation Parameters for the Comparative Study

Parameter	Value	Purpose
DC-link voltage, V_{dc}	400 V	Common inverter supply
Fundamental frequency, f_1	50 Hz	Reference output frequency
Carrier frequency, f_c	5 kHz	Equal switching-frequency basis
Modulation index, m	0.90	Common linear operating point
Load per phase	$10 \Omega + 20 \text{ mH}$	Balanced three-phase RL load
Simulation step	$2 \mu\text{s}$	Captures switching events accurately
Evaluation window	Last 5 cycles	Avoids start-up transient bias

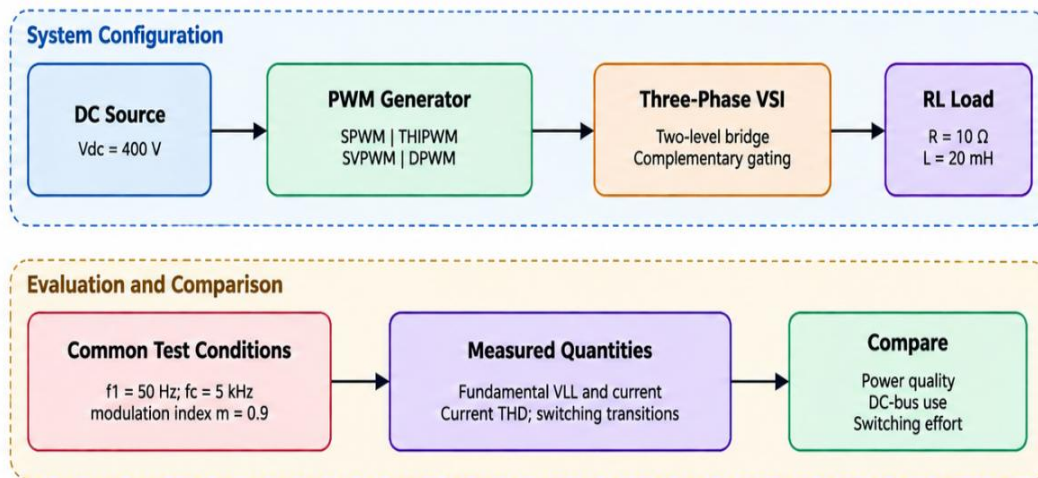


Figure 1. illustrates the common inverter model, identical test conditions, and the performance metrics applied to every PWM technique.

3. Electrical Model and Performance Measures

The upper-device gate state of each phase is obtained by comparing the normalized phase reference with the carrier. The pole voltage is then either $+V_{dc}/2$ or $-V_{dc}/2$. Because the load neutral is floating, the instantaneous phase voltage is calculated by subtracting the average of the three pole voltages from each pole voltage. The RL current is obtained from $di/dt = (v_{phase} - Ri)/L$ using forward time integration. Only the last five fundamental cycles are used for performance calculations so that start-up transients do not influence the comparison.

The first performance measure is the RMS magnitude of the 50 Hz fundamental component of line-to-line voltage, obtained from the discrete Fourier transform. The second is the 50 Hz fundamental RMS phase current. Current THD is calculated as $THD = [\sqrt{(I_2^2 + I_3^2 + \dots)}/I_1] \times 100\%$, equivalently using the total AC RMS after removing the fundamental component. The fourth measure is switching activity, counted as the number of upper-gate state changes per phase leg per fundamental cycle. Finally, theoretical linear DC-bus utilization is recorded. For SPWM the maximum sinusoidal modulation index is 1.0, while zero-sequence-injected methods can extend the linear fundamental command to approximately $2/\sqrt{3} = 1.1547$, corresponding to a 15.47% increase in available fundamental voltage.

4. Comparative Evaluation Procedure

Step 1: Define the common DC link, balanced RL load, fundamental frequency, carrier frequency, modulation index, and numerical time step listed in Table 1. Step 2: Generate three sinusoidal phase references separated by 120° . Step 3: construct the SPWM, THIPWM, SVPWM, and DPWM reference signals using the equations

above. Step 4: compare each normalized reference with the same 5 kHz triangular carrier to obtain complementary gate commands. Step 5: reconstruct pole voltages, line voltages, load-neutral phase voltages, and the three phase currents. Step 6: discard the initial transient and retain the last five 50 Hz cycles. Step 7: perform Fourier analysis to extract the 50 Hz fundamental values and current THD. Step 8: count switching transitions per phase leg. Step 9: compare the techniques using the same metrics and interpret the result in relation to prior PWM literature.

The principal validity control in this methodology is equality of operating conditions. The same DC supply, load, carrier, fundamental frequency, modulation command, integration step, and analysis window are used for all methods. Consequently, differences in current THD and switching activity are attributable to PWM sequence formation rather than to unequal test settings. The use of a carrier-equivalent SVPWM also avoids comparing different sampling mechanisms, which is important because carrier sampling itself can alter the harmonic spectrum (Hava et al., 1999).

Results

Table 2 summarizes the numerical results at $m = 0.9$. All four methods produce essentially the same 50 Hz line-to-line fundamental voltage (about 220 V RMS), confirming that the comparison is performed at the same commanded output. Differences appear primarily in harmonic current and switching activity. SVPWM gives the lowest simulated phase-current THD at 0.81%, followed by THIPWM at 0.84% and SPWM at 0.93%. The representative DPWM case produces 1.12% current THD, but its average gate transitions fall to about 133 per phase leg per fundamental cycle compared with 200 for the three continuous carrier methods.

Table 2. Comparative Results at $m = 0.9$

Technique	VLL,1 RMS (V)	I1 RMS (A)	Current THD (%)	Transitions/leg/cycle	Linear m max
SPWM	220.61	10.787	0.93	200	1.000
THIPWM	220.74	10.800	0.84	200	1.155
SVPWM	220.96	10.799	0.81	200	1.155
DPWM (upper-clamp)	220.01	10.760	1.12	133	1.155*

Conclusion and Discussion

This study developed a reproducible methodology for comparing four PWM approaches for a two-level, three-phase VSI using identical electrical and numerical conditions. The

results support three main conclusions. First, centered SVPWM provides the best current waveform quality among the tested methods at the common operating point, with simulated phase-current THD of 0.81%, while THIPWM gives nearly the same performance at 0.84%.

Second, zero-sequence injection allows THIPWM and SVPWM to use the DC link more effectively than classical SPWM; the theoretical linear fundamental range increases by approximately 15.47%. Third, a discontinuous clamping strategy can substantially reduce switching activity—about one third in the present implementation—although this benefit is accompanied by a modest increase in load-current distortion. The findings should not be interpreted as proving that one PWM technique is universally superior. SPWM remains the simplest option for low-cost digital or analog implementation. THIPWM is attractive when designers want much of the voltage-utilization benefit of SVPWM with a carrier-based structure. SVPWM is preferred where high DC-bus utilization, low harmonic current, and flexible switching-state control justify additional computation. DPWM becomes attractive when semiconductor switching loss and thermal stress are more important than minimizing current ripple. These conclusions align with the broader literature showing that carrier-based and space-vector methods are closely related and that performance is determined by zero-sequence selection, switching sequence, and clamping policy rather than by nomenclature alone (Wang, 2002; Yao et al., 2008). The main limitation is the use of ideal switches and a balanced RL load; dead time, device voltage drop, nonlinear machine impedance, common-mode voltage, thermal losses, and acoustic effects are not included. A future extension should implement the same four techniques on a DSP or FPGA-controlled inverter and measure semiconductor loss, common-mode voltage, motor current THD, and efficiency over a range of modulation indices and power factors. Nevertheless, the present methodology provides a compact, controlled baseline suitable for comparative PWM research and teaching.

References

- Binojkumar, A. C., Saritha, B., & Narayanan, G. (2016). Experimental comparison of conventional and bus-clamping PWM methods based on electrical and acoustic noise spectra of induction motor drives. *IEEE Transactions on Industry Applications*, 52(5), 4061–4073. DOI: 10.1109/TIA.2016.2584578.
- Hava, A. M., Kerkman, R. J., & Lipo, T. A. (1998). A high-performance generalized discontinuous PWM algorithm. *IEEE Transactions on Industry Applications*, 34(5), 1059–1071. DOI: 10.1109/28.720446.
- Hava, A. M., Kerkman, R. J., & Lipo, T. A. (1999). Simple analytical and graphical methods for carrier-based PWM-VSI drives. *IEEE Transactions on Power Electronics*, 14(1), 49–61. DOI: 10.1109/63.737592.
- Holmes, D. G. (1992). The general relationship between regular-sampled pulse-width-modulation and space vector modulation for hard switched converters. *Conference Record of the 1992 IEEE Industry Applications Society Annual Meeting*, 1002–1009. DOI: 10.1109/IAS.1992.244437.
- McGrath, B. P., Holmes, D. G., & Lipo, T. A. (2003). Optimized space vector switching sequences for multilevel inverters. *IEEE Transactions on Power Electronics*, 18(6), 1293–1301. DOI: 10.1109/TPEL.2003.818827.
- Van der Broeck, H. W., Skudelny, H.-C., & Stanke, G. V. (1988). Analysis and realization of a pulsewidth modulator based on voltage space vectors. *IEEE Transactions on Industry Applications*, 24(1), 142–150. DOI: 10.1109/28.87265.
- Wang, F. (2002). Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters. *IEEE Transactions on Industry Applications*, 38(2), 500–506. DOI: 10.1109/28.993172.
- Yao, W., Hu, H., & Lu, Z. (2008). Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter. *IEEE Transactions on Power Electronics*, 23(1), 45–51. DOI: 10.1109/TPEL.2007.911865.
- Zhou, K., & Wang, D. (2002). Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis. *IEEE Transactions on Industrial Electronics*, 49(1), 186–196. DOI: 10.1109/41.982262.