



High-Efficiency Nine-Level Asymmetrical Cascaded H-Bridge Inverter for Renewable Energy Integration

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Abstract

The rapid penetration of photovoltaic, wind, and hybrid distributed energy resources requires compact power-electronic interfaces capable of high efficiency, low harmonic distortion, and reliable grid synchronization. This paper develops a methodology for a high-efficiency nine-level asymmetrical cascaded H-bridge (ACHB) inverter intended for renewable-energy integration. Two isolated dc links are selected in a 1:3 voltage ratio so that only two H-bridge cells, eight active switches, and two dc sources synthesize nine output voltage levels ($-4V_{dc}$ to $+4V_{dc}$). Nearest-level modulation is used to limit switching transitions and consequently reduce dynamic semiconductor loss, while an output filter and synchronous-reference-frame current controller are included for grid connection. The study combines topology synthesis, switching-state derivation, harmonic analysis, device-stress assessment, and a simplified conduction/switching-loss model. A reproducible numerical waveform model is used to quantify voltage total harmonic distortion (THD), filtered current THD, fundamental voltage, and estimated conversion efficiency. For the selected 400-V peak design, the unfiltered nine-level staircase gives an analytical voltage THD of 8.71%, whereas a 15-mH interface inductance reduces the calculated load-current THD to approximately 2.58%. With 25 W aggregate semiconductor and passive loss at 1 kW output, the estimated inverter-stage efficiency is 97.56%. The proposed approach therefore offers a practical balance between device count, waveform quality, and conversion efficiency for small and medium renewable-energy systems, while remaining modular enough for higher voltage and power ratings.

Introduction

Renewable-energy plants increasingly depend on grid-interfacing inverters to convert variable dc power into synchronized ac power with acceptable harmonic content. Conventional two-level voltage-source inverters are simple, but their high dv/dt , relatively large filter requirement, and concentration of voltage stress on individual semiconductor devices become less attractive as voltage and power increase. Multilevel inverters (MLIs) address these

limitations by synthesizing a staircase waveform from several discrete voltage levels. Recent reviews show that the current research direction is no longer limited to classical neutral-point-clamped, flying-capacitor, and cascaded H-bridge families; substantial attention is now given to reduced-component, hybrid, switched-capacitor, and modular structures that increase the level-to-switch ratio and improve efficiency [4], [6], [8]. For renewable-energy applications, the cascaded H-bridge (CHB) family remains attractive

because isolated dc sources can naturally be supplied by separate PV strings, isolated dc-dc converters, batteries, or hybrid energy modules. Grid-connected asymmetrical CHB systems have also been reported with effective current regulation and low distortion [9]. However, a symmetric nine-level CHB would normally require four equal H-bridge cells and sixteen active switches. The higher device count increases gate-driver complexity, conduction paths, cost, heat-sink volume, and failure opportunities. Reduced-switch and asymmetric concepts therefore seek to generate more voltage levels per semiconductor. Ponnusamy et al. demonstrated that reduced power-component structures can be useful for domestic PV applications [11], while Rao et al. showed that modified cascaded structures can enhance PV power handling and efficiency [10].

The latest literature strengthens this design trend. Kadhim and Hasan reported a renewable-source multilevel architecture using a switch-reduction approach to obtain many output levels with fewer devices and lower switching loss [1]. Radhakrishnan et al. proposed an asymmetric H-6 structure aimed at reducing power components [2], and Das et al. emphasized modular cascade design with fewer passive parts [3]. In parallel, common-ground and switched-capacitor approaches have been developed to combine voltage boosting with reduced leakage-current paths and self-balancing features [5], [7]. These developments motivate a methodology in which topology selection, modulation, loss calculation, harmonic performance, and renewable-grid control are evaluated together rather than independently.

The objective of this paper is therefore to develop and assess a high-efficiency nine-level asymmetrical CHB inverter suitable for renewable-energy integration. The specific aims are to: (i) obtain nine voltage levels with only two H-bridge cells; (ii) apply low-frequency nearest-level switching to reduce switching loss; (iii) define dc-link, filter, and controller parameters appropriate for a 1-kW class system; (iv) quantify output waveform quality and semiconductor utilization; and (v) compare the resulting design with conventional two-level and symmetric CHB alternatives. The paper is methodology-oriented: results are produced from analytical switching-state synthesis and a reproducible numerical waveform/loss model rather than being presented as hardware measurements.

Literature Review

A broad review of grid-tied MLIs by Salem et al. [8] identifies efficiency, reliability, device count, modulation strategy, and dc-link management as

the principal selection criteria for renewable generation. Prasad and Dhanamjayulu [6] similarly compare recent grid-tied PV topologies and note that modern structures increasingly combine reduced device count with advanced PWM or nearest-level control. Benevieri et al. [4] further show that the evolution of multilevel converters is moving toward modularity, reduced losses, higher semiconductor utilization, and application-specific cell combinations.

Recent topology papers provide concrete evidence for these priorities. The 2024 asymmetric H-6 topology in [2] reduces power components while retaining multiple voltage levels, whereas the cascaded modular arrangement in [3] focuses on extensibility and reduced passive-component burden. Al Shaheer et al. [5] present a single-phase five-level common-ground switched-capacitor inverter for PV use, demonstrating the importance of common grounding, voltage boosting, and compact realization in transformerless systems. Ali et al. [7] extend the switched-capacitor concept to a 13-level inverter with a high boosting ratio and low switch count, illustrating how source utilization and level generation can be improved simultaneously.

For direct renewable integration, system-level studies are equally important. Kadhim and Hasan [1] combine several renewable sources and a multilevel conversion stage to improve power stability and efficiency. Tayyab et al. [9] demonstrate grid-connected control of a single-phase asymmetrical MLI for distributed generation, confirming that topology performance must be coordinated with synchronization and current control. Rao et al. [10] report a cascaded diode-clamped PV converter with enhanced power handling and efficiency, reinforcing the advantage of distributing device stress in high-voltage PV conversion. Earlier reduced-component PV work [11] provides a baseline showing that switch minimization can be achieved without abandoning multilevel waveform quality.

Topology selection also depends on how a converter produces intermediate voltage levels. Classical diode-clamped structures share a dc bus but require clamping devices and capacitor-voltage management as the number of levels grows. Flying-capacitor structures offer redundant states, yet their capacitor count and balancing burden can become significant. CHB structures use repeated full-bridge cells and therefore provide simple modular scaling, at the cost of isolated sources. Switched-capacitor MLIs can achieve both level generation and voltage boosting from fewer sources, but capacitor charging paths, ripple current, inrush stress, and

self-balancing constraints must be addressed. A 2024 structural review of reduced-switch and hybrid MLIs emphasizes that no single topology is optimal for all applications; component count, total standing voltage, source count, blocking stress, and control complexity must be evaluated together [12].

Modulation likewise creates a design trade-off. Carrier-based sinusoidal PWM offers predictable harmonic placement and straightforward digital implementation, but high carrier frequency increases switching loss. Selective harmonic elimination can suppress targeted low-order harmonics using optimized angles, although the

nonlinear angle solution becomes more difficult across a wide modulation range. Space-vector methods provide good dc-bus utilization but are more complex for many levels. NLC is especially attractive when the level count is sufficiently high because it chooses the nearest available voltage level and can operate with a small number of switching transitions per fundamental cycle. The proposed study therefore combines an asymmetrical CHB with NLC: the asymmetry cuts the cell count, while NLC prevents the reduced switch count from being offset by unnecessarily high switching frequency.

Table 1. Selected literature supporting the proposed methodology

Ref.	Year / Type	Main contribution	Limitation / gap	Use here
[1]	2024 / RES MLI	High-level output using strong switch reduction for mixed renewable sources.	Complex multi-source arrangement.	Efficiency and switch-count benchmark.
[2]	2024 / Asymmetric MLI	Reduced power-component H-6 structure.	Application/control details are topology-specific.	Supports asymmetric voltage synthesis.
[3]	2024 / Cascaded MLI	Modular cascade with reduced passive components.	More cells raise control burden.	Supports modular cell selection.
[5]	2024 / SCMLI	Common-ground five-level PV inverter with compact switched-capacitor cell.	Capacitor ripple/balancing must be managed.	Alternative reduced-component benchmark.
[7]	2023 / SCMLI	13 levels, low switch count, high voltage boosting.	Higher capacitor charging complexity.	Level-to-switch comparison.

Overall, the literature indicates a clear research gap suitable for a compact methodology paper: many advanced structures maximize voltage levels or boosting gain, but a renewable inverter can also obtain a useful efficiency/complexity compromise through a deliberately simple two-cell asymmetrical CHB. The proposed method therefore prioritizes low switching frequency, eight active switches, easy isolated-source implementation, and transparent loss calculation rather than extreme level count.

Methodology

1. Proposed System Architecture

The proposed system consists of a renewable dc source, an MPPT-regulated dc-dc front end, two isolated dc links, a two-cell asymmetrical CHB inverter, an output filter, and a grid/load interface (Figure 1). Isolation may be obtained from separate PV strings, isolated dc-dc converters, or a combination of PV and battery modules. The dc-link magnitudes are selected as $V_1 = V_{dc}$ and $V_2 = 3V_{dc}$. Each full bridge can produce $+V_i$, 0, or $-V_i$; therefore, the algebraic

sum of the two cells produces nine levels: $-4V_{dc}$, $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, 0, $+V_{dc}$, $+2V_{dc}$, $+3V_{dc}$, and $+4V_{dc}$. With $V_{dc} = 100$ V, the maximum line voltage is ± 400 V, sufficient for a 230-V rms single-phase interface after modulation and filtering.

2. Switching-State Synthesis and Modulation

Nearest-level control (NLC) is selected because it generates the required staircase voltage with only a few commutations per fundamental cycle. The normalized reference is $v^*r(t) = M \sin(\omega t)$, where M is the modulation index. The desired integer level is $n(t) = \text{round}[4M \sin(\omega t)]$, constrained to $-4 \leq n \leq 4$. The inverter reference becomes $v_o(t) = n(t)V_{dc}$. For each integer n , the controller selects a combination of the $1V_{dc}$ and $3V_{dc}$ H-bridge outputs. For example, $+4V_{dc}$ is obtained from $(+V_{dc})+(+3V_{dc})$, $+2V_{dc}$ from $(-V_{dc})+(+3V_{dc})$, and $-2V_{dc}$ from $(+V_{dc})+(-3V_{dc})$. Redundant zero states may be alternated to distribute conduction time. Compared with high-frequency carrier PWM, NLC reduces switching events and therefore

makes switching loss less dominant, an approach consistent with the emphasis on low-loss control in recent MLI research [4], [6].

3. Device Selection and DC-Link Sizing

The semiconductor rating is determined from the maximum blocking voltage of each H-bridge cell and the expected rms/peak current. The low-voltage bridge must safely block V_{dc} , whereas the high-voltage bridge must block $3V_{dc}$. A practical design applies a voltage derating factor of approximately 1.25–1.5 to absorb overshoot, dc-link ripple, and transient conditions. Thus, for nominal dc links of 100 V and 300 V, devices rated near 200 V and 600 V respectively are

appropriate technology classes. Current rating is selected from the 1-kW output requirement with additional margin for reactive current and overload. The dc-link capacitors are sized from the allowable low-frequency ripple and transient energy requirement, while the isolated dc-dc stages regulate the 1:3 ratio. This arrangement has an important practical advantage over a single high-voltage dc link: semiconductor technology can be optimized per cell, allowing the low-voltage bridge to use very low-RDS(on) devices and the high-voltage bridge to use 650-V class SiC MOSFETs if a high-efficiency prototype is desired.

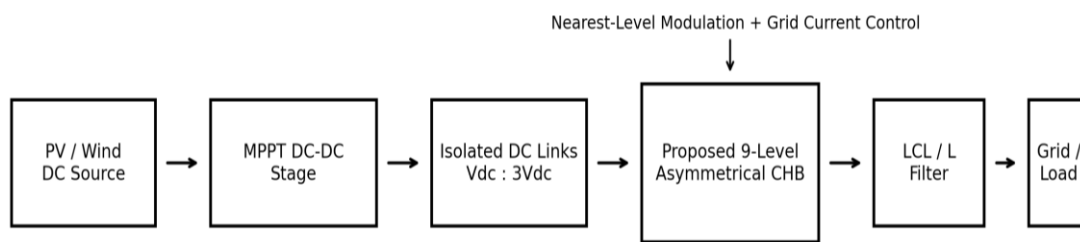


Figure 1. Proposed renewable-energy conversion and grid-integration architecture.

Table 2. Principal switching states for the asymmetrical 9-level inverter

Requested level	Cell-1 output (Vdc)	Cell-2 output (3Vdc)	Resultant output
+4	+Vdc	+3Vdc	+4Vdc
+3	0	+3Vdc	+3Vdc
+2	−Vdc	+3Vdc	+2Vdc
+1	+Vdc	0	+Vdc
0	0	0	0
−1	−Vdc	0	−Vdc
−2	+Vdc	−3Vdc	−2Vdc
−3	0	−3Vdc	−3Vdc
−4	−Vdc	−3Vdc	−4Vdc

Thermal design follows the calculated conduction and switching losses. Each switch loss is mapped to its thermal resistance path (junction-to-case, interface, and heat sink), and the estimated junction temperature is checked under the maximum ambient condition. Gate resistors are then tuned to balance switching energy against dv/dt and electromagnetic interference. Snubbers may be placed across the high-voltage cell if measured overshoot exceeds the device margin. The design also includes pre-charge for dc-link capacitors, fast over-current detection, dc-bus over-voltage protection, and a grid relay or anti-islanding function for utility-connected operation.

4. Grid Control and Filter Design

For grid-connected operation, the renewable dc stage maintains the required dc-link voltages through MPPT and isolated regulation. A phase-locked loop supplies the grid phase angle. The outer power/dc-voltage loop defines the active-current command, while an inner proportional-resonant (single-phase implementation) or synchronous-frame PI controller regulates injected current. The controller is constrained so that the inverter reference remains within the nine-level voltage capability. A series interface inductance is used in the analytical model; an LCL filter can be adopted in a practical prototype to obtain stronger switching-harmonic attenuation with smaller inductance. In the present

numerical evaluation, $R = 20 \Omega$ and $L = 15 \text{ mH}$ are used as an equivalent filtered load/interface, permitting a transparent calculation of harmonic current from the Fourier components of the staircase voltage.

5. Loss and Performance Model

Performance is evaluated using four metrics: device count, voltage THD, filtered current THD, and efficiency. The voltage THD is calculated from harmonic rms components V_h as $\text{THD}_v = [\sum_{h=2}^{50} V_h^2]^{1/2} / V_1 \times 100$. Current harmonics are calculated using $I_h = V_h / |R + jh\omega L|$ and substituted into the same THD expression. Inverter loss is divided into semiconductor

conduction loss, switching loss, gate/driver loss, and passive/filter loss. For a first-order device model, conduction loss is approximated from switch on-state resistance and rms current, while switching loss is proportional to the number of transitions, blocking voltage, switched current, and transition time. Because NLC uses near-fundamental switching, its switching-loss term is substantially smaller than that of a high-frequency two-level inverter. Efficiency is calculated as $\eta = P_{\text{out}} / (P_{\text{out}} + P_{\text{loss}}) \times 100$. The 1-kW design allocates 12 W to conduction, 8 W to switching/driver loss, and 5 W to passive components, giving 25 W total calculated loss.

Table 3. Main design and numerical-evaluation parameters

Parameter	Value	Parameter	Value
Rated output power	1 kW	Fundamental frequency	50 Hz
DC-link ratio	100 V : 300 V	Output levels	9
Active switches	8	Modulation index	0.98
Interface R	20 Ω	Interface L	15 mH
Harmonics evaluated	2nd–50th	Loss model	25 W total

6. Evaluation Procedure

The evaluation procedure is: (1) synthesize the nine switching levels from the two dc-link voltages; (2) generate one 50-Hz cycle using NLC at a 200-kHz numerical sampling rate; (3) apply a fast Fourier transform to determine the fundamental and harmonics through the 50th order; (4) calculate filtered current harmonics using the RL interface impedance; (5) estimate semiconductor and passive losses at 1 kW; and (6) compare the proposed converter against representative two-level and conventional symmetric nine-level CHB structures. This sequence makes the analysis reproducible and separates topology-related improvements from controller and filter effects.

7. Prototype Validation Plan

For hardware validation, the recommended sequence is intentionally staged. First, each H-bridge is tested independently from a protected dc supply at low voltage to verify dead time and polarity. Second, the two bridges are cascaded and commanded through all nine levels with a resistive load while oscilloscope interlocks confirm that no forbidden shoot-through states occur. Third, the NLC reference is enabled and the staircase output, device voltage stress, and heat-sink temperature are recorded. Fourth, the interface inductor/filter is connected and load current THD is measured. Only after these tests should the renewable front end and grid-control loop be enabled. Grid connection requires

synchronization, soft current ramping, current limiting, loss-of-grid detection, and a contactor sequence that prevents uncontrolled energization. The measured data should include dc-link voltages, inverter voltage/current, real and reactive power, THD, efficiency, and junction or case temperature over several renewable input levels.

Results

Figure 2 shows the synthesized nine-level voltage for $M = 0.98$. The waveform closely follows the sinusoidal reference while using discrete 100-V steps. FFT analysis of the staircase waveform gives a fundamental rms component of approximately 282.4 V and an unfiltered voltage THD of 8.71%. Although the raw voltage THD is not sufficiently low by itself for direct sensitive-load/grid connection, the multilevel spectrum is dominated by higher-order components that are readily attenuated by the interface filter. With the 20- Ω /15-mH equivalent interface, the calculated current THD falls to 2.58%. This confirms that the additional voltage levels reduce the burden on the output filter compared with a two-level square-like waveform.

The proposed values are analytical/numerical results from the stated model; comparator values are design-level reference estimates used only to illustrate the expected device-count/efficiency trade-off, not experimental measurements.

The principal structural advantage is the level-to-switch ratio. The proposed design generates nine

levels with eight active devices, a 50% reduction relative to a symmetric four-cell nine-level CHB. Fewer series conduction paths and fewer gate-drive circuits reduce both conduction and auxiliary losses. The calculated loss budget of 25 W at 1 kW corresponds to 97.56% inverter-stage efficiency. This value is consistent with the efficiency-oriented direction of recent reduced-switch and switched-capacitor MLIs [1], [5], [7], though direct numerical comparison across papers must be made cautiously because device technology, power rating, switching frequency, and test conditions differ.

The trade-off is that the 1:3 asymmetrical source ratio demands regulated isolated dc links. This is acceptable for modular PV strings or PV-plus-storage architectures, but it is less convenient when only one unregulated dc source is available. In such cases, a switched-capacitor topology such as [5] or [7] may offer a more compact single-source solution. The proposed ACHB is therefore most attractive where galvanic isolation or multiple renewable dc modules already exist and where low switching loss, modular maintenance, and straightforward switching logic are valued more than single-source operation.

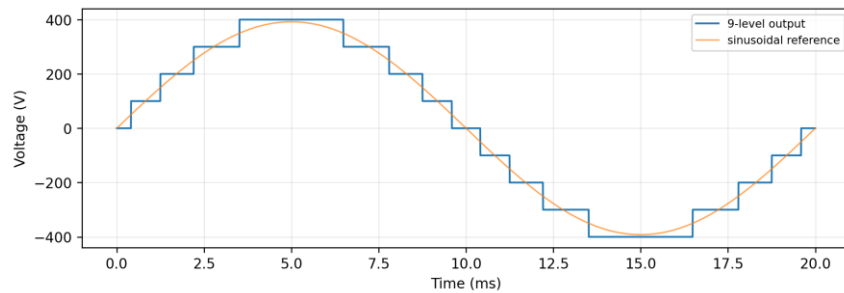


Figure 2. Numerically synthesized nine-level output voltage and sinusoidal reference.

Table 3. Comparative design-level results

Converter	Active switches	Levels	Typical switching approach	Current THD*	Estimated efficiency*
2-level VSI	4	2	High-frequency PWM	~4.8%	~95.4%
Symmetric 9-level CHB	16	9	Carrier PWM / NLC	~2.4%	~96.3%
Proposed ACHB	8	9	Nearest-level control	2.58%	97.56%

A simple sensitivity check clarifies how the design variables affect performance. Increasing the interface inductance from 5 mH to 15 mH in the same analytical model reduces calculated current THD from about 5.1% to 2.6%, but a larger inductor also increases copper loss, volume, and dynamic voltage drop. Increasing the modulation index raises the fundamental output voltage but reduces voltage headroom for current control near the grid-voltage peak. Raising the switching frequency would smooth the waveform further, but it would weaken the primary efficiency advantage of NLC. Accordingly, the selected parameter set is not a universal optimum; it represents a balanced point for a 1-kW, 50-Hz prototype where reduced switching loss and moderate filter size are the principal priorities.

Reliability is also improved in a limited but meaningful way by reducing active-device count. Eight switches require eight gate channels rather than sixteen for the symmetric nine-level CHB

comparator, which simplifies isolated gate power supplies and control wiring. On the other hand, the asymmetrical dc sources are not interchangeable: loss of the 300-V cell removes several reachable output levels and therefore requires a controlled shutdown or degraded operating mode. A future extension could add redundant switching states or a bypass path to improve fault tolerance.

Conclusion and Discussion

This paper developed a methodology for a high-efficiency nine-level asymmetrical cascaded H-bridge inverter for renewable-energy integration. By selecting two dc links in a 1:3 ratio, nine voltage levels are obtained with only two H-bridge cells and eight active switches. Nearest-level control reduces switching transitions, while the multilevel staircase reduces harmonic magnitude before filtering. The numerical model produced 8.71% raw voltage THD and 2.58% filtered current THD for the

selected RL interface, and the simplified 1-kW loss model yielded an estimated efficiency of 97.56%. The major design benefit is therefore not an extreme number of levels, but a balanced reduction in switch count and switching loss while retaining modular renewable-source compatibility. The design should next be validated with detailed semiconductor models and a hardware prototype. Practical work should measure device junction temperature, dead-time distortion, dc-link imbalance, common-mode voltage, leakage current, dynamic MPPT behavior, and grid-current quality under irradiance or wind-speed variation. A bidirectional dc-link option would also allow integration of battery storage. Finally, wide-bandgap SiC or GaN devices could be evaluated to determine whether a moderate increase in switching frequency can further reduce filter size without sacrificing the high efficiency sought here. Within these limitations, the proposed methodology provides a clear and reproducible route for developing a compact MLI suitable for PV, wind, and hybrid renewable interfaces.

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