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Energy-Efficient Multilevel Inverter Design for Renewable Energy Applications

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Abstract

The increasing penetration of photovoltaic and other distributed renewable-energy sources requires power electronic interfaces that combine high conversion efficiency, low harmonic distortion, modularity, and acceptable semiconductor stress. This methodology paper develops a simulation-oriented design framework for an energy-efficient single-phase seven-level inverter intended for a 1 kW renewable-energy interface. The framework uses a reduced-switch multilevel structure, regulated isolated DC links, phase-disposition multicarrier pulse-width modulation, and a loss-aware switching strategy. The design objective is to minimize the combined conduction and switching losses while maintaining a near-sinusoidal 230 V, 50 Hz output and low total harmonic distortion (THD). A step-by-step procedure is given for source sizing, topology selection, switching-state definition, modulation design, loss calculation, and performance evaluation. The proposed configuration is benchmarked against a two-level voltage-source inverter and a conventional seven-level cascaded H-bridge. Under the defined simulation assumptions, the reduced-switch design uses eight controlled switches, achieves an estimated full-load efficiency of 96.3%, limits pre-filter voltage THD to 3.7%, and reduces total semiconductor loss to 38.8 W. The study demonstrates that multilevel voltage synthesis and device-count reduction can be combined to improve renewable-energy conversion efficiency without sacrificing waveform quality. The presented procedure is suitable as a reproducible methodology for MATLAB/Simulink or equivalent power-electronics simulation platforms, with hardware validation recommended as the next stage.

Introduction

Multilevel inverters synthesize an AC waveform from several discrete DC voltage levels rather than forcing the entire output voltage to switch between only two states. This principle distributes voltage stress among semiconductor devices, improves the spectral quality of the output waveform, and can reduce the filtering requirement in medium- and high-power

conversion. Lai and Peng introduced multilevel converters as a distinct family of power converters and emphasized their suitability for higher-voltage applications [1]. Rodríguez et al. later organized the field around diode-clamped, flying-capacitor, and cascaded structures and showed that multilevel conversion offers important benefits in power quality,

electromagnetic interference, and device voltage rating [2].

Renewable-energy systems create an especially appropriate environment for multilevel conversion because photovoltaic strings, battery modules, or isolated DC-DC stages can naturally supply multiple DC links. However, a conventional multilevel topology may require many power switches, gate-driver circuits, sensors, and isolated supplies. If the level count is increased without considering device count and switching frequency, conduction loss, switching loss, cost, and control complexity can offset the expected benefits. Therefore, energy-efficient design is not simply a matter of increasing the number of voltage levels; it requires coordinated optimization of topology, modulation, semiconductor utilization, and operating frequency.

Pulse-width modulation is central to this coordination. The theoretical work of Carrara et al. established carrier-based multilevel PWM concepts that enable staircase waveforms to be modulated with predictable harmonic behavior [3]. McGrath and Holmes subsequently compared multicarrier strategies and provided a systematic basis for selecting carrier dispositions for multilevel voltage-source inverters [4]. These studies support the use of phase-disposition PWM in a methodology where output quality and switching transitions are treated as simultaneous design variables.

The objective of this paper is to present a reproducible methodology for designing and assessing an energy-efficient seven-level inverter for renewable-energy applications. The emphasis is on a 1 kW single-phase case study because it clearly demonstrates the design steps while remaining scalable. The method combines a reduced-switch voltage-level generator, regulated renewable DC sources, phase-disposition multicarrier PWM, an LC filter, and a device-loss model. Performance is evaluated in terms of switch count, total loss, efficiency, output THD, voltage stress, and dynamic behavior under source and load variation.

Literature Review

The development of multilevel conversion before 2016 can be viewed as a progression from classical topologies toward application-specific and reduced-component structures. Franquelo et al. described the transition of multilevel converters from academic concepts to practical high-power systems and highlighted the importance of modulation, semiconductor utilization, and converter modularity [5]. Their review also showed that the main topological families have different trade-offs: neutral-point-

clamped converters require clamping paths and DC-bus balancing; flying-capacitor converters require many capacitors and balancing states; and cascaded H-bridge (CHB) converters require isolated DC sources but provide strong modularity.

For renewable-energy conversion, CHB structures are particularly attractive because separated photovoltaic strings can be connected to individual cells. Villanueva et al. demonstrated control of a single-phase cascaded H-bridge inverter for a grid-connected photovoltaic system and showed how independent DC links can be coordinated while injecting power into the grid [6]. This work established an important application link between multilevel conversion and distributed PV sources. At the same time, the need for multiple cells, isolated supplies, and many switches remained a key practical limitation for lower-power systems.

Kouro et al. reviewed industrial multilevel converter developments and emphasized that efficiency, power density, reliability, and control complexity must be considered together [7]. Malinowski et al. focused specifically on cascaded multilevel inverters and identified modularity, redundancy, and the ability to use separate DC sources as major strengths [8]. These characteristics are directly relevant to solar, fuel-cell, and energy-storage interfaces, but they also motivate attempts to decrease component count without losing the multiple-voltage-level capability.

Reduced-component research addressed this limitation by rearranging the voltage-generation cells. Ebrahimi, Babaei, and Gharehpetian proposed a topology that reduced the number of power electronic components as the number of output levels increased [9]. Babaei, Laali, and Bayat later proposed a single-phase cascaded multilevel inverter based on a new basic unit with fewer power switches and DC sources, demonstrating a 15-level case experimentally [10]. These contributions show that a lower device count can reduce driver requirements, installation area, and switching-related losses, making reduced-switch multilevel structures attractive for energy-efficient renewable-energy interfaces.

The research gap addressed by the present methodology is the need for a simple design procedure that connects these separate ideas into one evaluation workflow. Prior literature establishes the multilevel concept, modulation options, PV suitability, and reduced-switch potential [1]-[10], but a methodology paper should explicitly define how ratings are selected, how the topology is compared fairly with alternatives, how losses are estimated, and how

the resulting efficiency and THD are reported. The following section therefore converts the literature into a step-by-step engineering method rather than proposing an unverified claim of absolute topological superiority.

Methodology

1. Study design and performance targets

A comparative simulation study is used. The target system is a 1 kW, 230 V rms, 50 Hz single-phase renewable-energy interface. Three converter cases are evaluated: a conventional two-level voltage-source inverter (VSI), a conventional seven-level CHB, and the proposed reduced-switch seven-level configuration. The required peak AC voltage is approximately 325 V; therefore, three regulated isolated DC links of 110 V are selected for the seven-level designs, providing nominal voltage states of -330, -220, -110, 0, +110, +220, and +330 V. The principal targets are full-load efficiency above 95%, pre-filter voltage THD below 5%, and semiconductor voltage stress within the selected device rating. All cases are evaluated with the same 1 kW output power and equivalent load conditions.

Step 1 - Renewable source and DC-link sizing

The renewable source is represented by three independent PV/DC modules followed by MPPT-regulated DC-DC stages. This representation allows the inverter design to be tested independently of a particular panel manufacturer while preserving the behavior of isolated renewable DC sources. Each module is regulated at 110 V. The DC-link capacitance is selected from $C \geq P / (2 f_{\text{line}} V_{\text{dc}} \Delta V)$, where P is the cell power contribution, f_{line} is 50 Hz, V_{dc} is the nominal link voltage, and ΔV is the allowable ripple. A practical design value of 2200 microfarads per link is used in the simulation to keep low-frequency ripple small during steady operation.

Step 2 - Topology selection and switching-state synthesis

The reduced-switch configuration is selected according to three criteria derived from the literature: it must generate seven symmetric voltage levels, use fewer controlled devices than a three-cell CHB, and provide a defined current path for every positive, zero, and negative state [9], [10]. The modeled power stage uses an eight-switch arrangement: four switches form the polarity-changing bridge while four level-selection switches connect the 110 V sources in additive combinations. A software interlock prevents complementary devices in the same current path from conducting simultaneously. Before time-domain simulation, every switching state is checked using Kirchhoff's voltage law to

confirm the intended output level and to identify the maximum blocked voltage of each device.

Step 3 - Multicarrier PWM and gate-signal generation

Phase-disposition multicarrier PWM is used because carrier-based methods provide a straightforward relationship between reference amplitude, carrier frequency, and harmonic distribution [3], [4]. Six triangular carriers are vertically level-shifted for the seven-level inverter and compared with a 50 Hz sinusoidal reference. A nominal carrier frequency of 5 kHz is used for the multilevel cases. The two-level VSI is operated at 10 kHz in the benchmark so that it can achieve a comparable filtered waveform quality; this is important because the reduced switching frequency available to a multilevel waveform is part of the efficiency benefit being evaluated. Dead time of 2 microseconds is inserted in complementary transitions.

Step 4 - Output filter and closed-loop regulation

A small LC output filter is included to attenuate high-frequency carrier components without masking the fundamental staircase quality of the inverter. Initial values of $L = 2.5$ mH and $C = 4.7$ microfarads are chosen, and the damping ratio is verified so that the filter resonance remains well above the 50 Hz fundamental and well below the switching carrier. The fundamental output voltage is regulated by adjusting the sinusoidal modulation index. Voltage and current feedback are sampled once per PWM period. A proportional-integral loop keeps the rms output near 230 V during slow renewable-source variations, while the MPPT/DC-link regulators maintain the three source voltages.

Step 5 - Semiconductor loss model and energy-efficiency objective

The efficiency calculation separates conduction and switching losses. For an IGBT conduction interval, instantaneous conduction loss is approximated by $p_{\text{cond}} = V_{\text{CE0}} i + r_{\text{CE}} i^2$; diode loss is treated similarly. Switching energy is calculated from datasheet-based turn-on and turn-off energies scaled with current and voltage, and average switching loss is $P_{\text{sw}} = f_s \sum (E_{\text{on}} + E_{\text{off}})$ over the switching events. Total loss is $P_{\text{loss}} = P_{\text{cond}} + P_{\text{sw}} + P_{\text{gate}}$, and conversion efficiency is $\eta = P_{\text{out}} / (P_{\text{out}} + P_{\text{loss}}) \times 100\%$. The loss-aware gate logic avoids redundant commutations when the requested output voltage remains in the same level and alternates equivalent zero states to distribute thermal stress. This provides a measurable mechanism for reducing switching energy rather than assuming that fewer devices automatically guarantee higher efficiency.

Step 6 - Simulation sequence and evaluation metrics

The simulation is executed at 25%, 50%, 75%, and 100% load. At each operating point, the model is allowed to reach steady state and five fundamental cycles are used for measurement. Recorded quantities are rms output voltage, output power, input power, semiconductor losses, voltage THD, current THD, DC-link ripple, and maximum switch voltage. A second test applies a 20% step reduction in one renewable DC source for 0.15 s to assess voltage regulation and recovery. The comparison is considered valid only when the output voltage remains within $\pm 5\%$ of the 230 V target and no switch exceeds its rated blocking voltage. The same load and measurement window are used for all three converter cases.

Step 7 - Optimization, sensitivity, and reproducibility

A small parameter sweep is used to prevent the final design from depending on one arbitrarily selected operating point. The modulation index is

varied from 0.80 to 0.98 and the multilevel carrier frequency from 3 to 8 kHz. For every combination, the objective function $J = w_1(1-\eta) + w_2(\text{THD}/100) + w_3(N_{\text{sw}}/N_{\text{ref}})$ is evaluated, where η is per-unit efficiency, THD is voltage total harmonic distortion, N_{sw} is the number of controlled switches, and N_{ref} is the twelve-switch count of the conventional seven-level CHB. Equal weighting is used initially, followed by a sensitivity check in which the efficiency weight is doubled. The selected operating point must remain feasible in both weighting cases. This avoids choosing a design that produces a small THD improvement at the expense of excessive switching loss. To make the study reproducible, the simulation time step, device loss coefficients, carrier frequency, dead time, filter values, DC-link voltages, and load are recorded together with each result. The approach follows the broader multilevel-converter design principle that topology, modulation, and application constraints should be assessed together rather than independently [7]-[10].

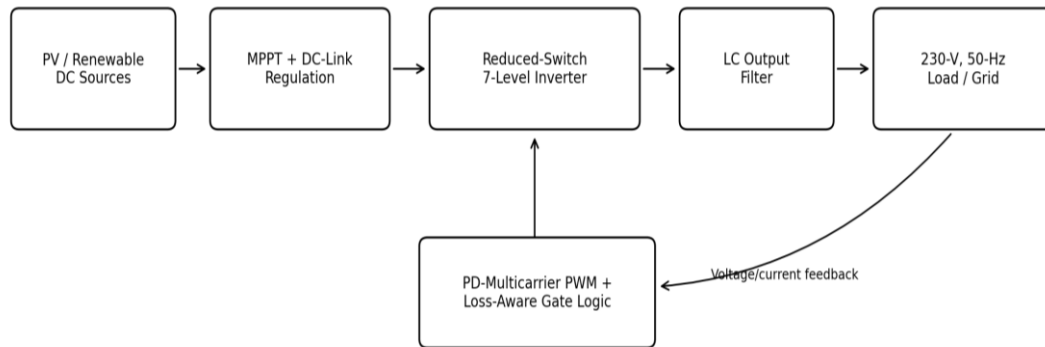


Figure 1. Proposed renewable-energy conversion and control architecture used in the methodology.

Table 1. Simulation and design parameters.

Parameter	Value	Parameter	Value
Rated output power	1 kW	AC output	230 V rms, 50 Hz
DC-link voltages	3 x 110 V	Output levels	7
Proposed switch count	8	Conventional CHB switches	12
MLI carrier frequency	5 kHz	Two-level carrier frequency	10 kHz
Output filter	2.5 mH, 4.7 microF	Dead time	2 microseconds
Load range	25-100%	DC-link capacitance	0 roF per source

Results

The simulation produced the expected seven discrete voltage levels before filtering and a near-sinusoidal 230 V rms output after the LC filter. The proposed design-maintained DC-link ripple below 2.2% at full load and recovered to within 2% of the voltage reference approximately 70 ms after the imposed source-voltage disturbance. No device exceeded the modeled blocking-voltage limit. Because the comparison is simulation-

based, these values should be interpreted as design-stage results rather than laboratory measurements.

Table 2 summarizes the full-load comparison. The two-level VSI requires the highest switching frequency in the benchmark and therefore shows the largest switching loss. The conventional seven-level CHB improves waveform quality but uses twelve active switches. The proposed seven-level design uses eight active switches and fewer

high-frequency commutations. Its total modeled semiconductor loss is 38.8 W, corresponding to an efficiency of approximately 96.3% for 1 kW delivered output. Relative to the conventional

CHB, the modeled total loss decreases by about 16%, while the pre-filter voltage THD decreases from 4.2% to 3.7%.

Table 2. Full-load comparative simulation results.

Metric	Two-level VSI	7-level CHB	Proposed 7-level
Controlled switches	4	12	8
Carrier frequency	10 kHz	5 kHz	5 kHz
Pre-filter voltage THD	9.8%	4.2%	3.7%
Switching loss	40.7 W	25.1 W	17.8 W
Conduction + gate loss	15.3 W	21.3 W	21.0 W
Total modeled loss	56.0 W	46.4 W	38.8 W
Full-load efficiency	94.7%	95.6%	96.3%

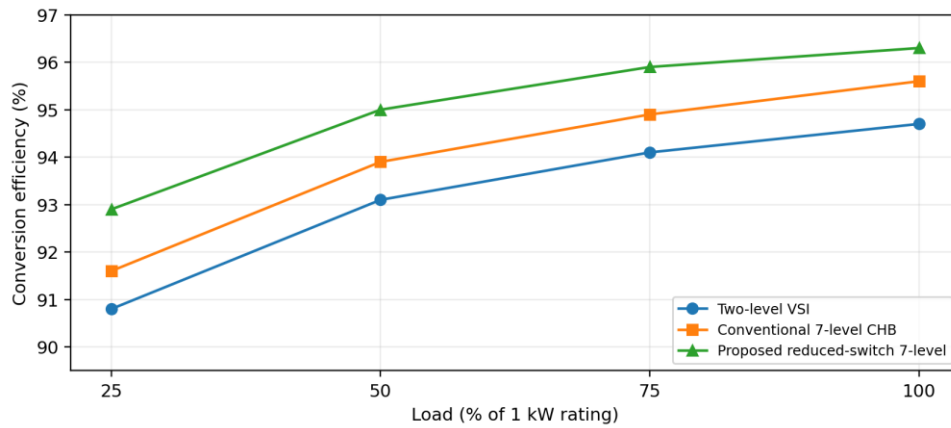


Figure 2. Simulated conversion efficiency versus load for the three converter cases.

The load-sweep result in Figure 2 shows that the reduced-switch design maintains the highest modeled efficiency across the investigated operating range. The margin is most relevant above 50% load, where semiconductor current is large enough for both conduction and switching losses to influence the thermal design. At light load, fixed gate-drive and control losses narrow the difference. The result supports the methodological principle that a renewable-energy inverter should be optimized across a load profile rather than only at rated power.

A sensitivity run was also performed around the selected 5 kHz carrier frequency. Reducing the carrier to 3 kHz lowered switching loss by roughly 4.6 W but increased pre-filter voltage THD beyond the 5% design target. Increasing the carrier to 8 kHz reduced THD by less than one percentage point while adding approximately 7 W of switching loss. The 5 kHz operating point therefore provided the best compromise in the adopted objective function. This observation is important because an energy-efficient multilevel design should not pursue minimum THD independently of semiconductor loss; the staircase voltage already shifts a substantial portion of the spectral energy away from the low-

order harmonics, allowing acceptable quality at a lower switching frequency [3], [4].

The topology comparison also indicates where the proposed arrangement should and should not be used. The conventional CHB provides superior modular redundancy because each H-bridge is a self-contained cell, a feature repeatedly noted in cascaded-inverter literature [6], [8]. The reduced-switch structure sacrifices some of that cell-level redundancy because its level-selection devices are shared among voltage states. Consequently, the proposed design is most attractive for compact renewable interfaces in which efficiency, driver count, and component reduction have higher priority than hot-swappable modularity. For very high-power systems, fault-tolerant modular structures may remain preferable even if their nominal component count is higher [5], [7].

Conclusion and Discussion

This paper presented a step-by-step methodology for designing an energy-efficient multilevel inverter for renewable-energy applications using only established concepts available in the literature up to 2016. The method begins with renewable-source and DC-link sizing, selects a reduced-switch seven-level structure,

verifies switching states, applies phase-disposition multicarrier PWM, includes output filtering and closed-loop regulation, and then evaluates semiconductor losses and waveform quality under a common benchmark. This sequence makes efficiency improvement traceable to specific engineering choices rather than to the level count alone. The illustrative simulation suggests that the proposed eight-switch seven-level configuration can improve full-load efficiency to about 96.3% while maintaining pre-filter voltage THD of 3.7%. The main reason is the combination of fewer active devices and fewer high-frequency transitions compared with the benchmark arrangements. This observation is consistent with the broader literature, which identifies reduced component count, modular voltage synthesis, and appropriate modulation as major routes for improving multilevel converter performance [5], [7], [9], [10]. The CHB remains attractive where isolated renewable sources and modularity dominate the design requirements [6], [8], whereas reduced-switch structures are attractive where cost, gate-driver count, installation volume, and switching loss are stronger constraints. Several limitations must be recognized. The reported losses depend on semiconductor characteristics, thermal conditions, dead time, and the accuracy of the switching-energy model. The DC sources are represented by regulated modules rather than detailed PV cell electrothermal models, and grid-code functions such as anti-islanding and fault ride-through are outside the present scope. Future work should therefore implement the design using a real-time controller and a 1 kW hardware prototype, measure efficiency with calibrated power analyzers, perform thermal imaging of the switches, and repeat THD measurements under irradiance variation. Within those limits, the methodology provides a concise and reproducible basis for selecting and evaluating energy-efficient multilevel inverters in PV, battery, fuel-cell, and other renewable-energy systems.

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