



Performance Evaluation of a Reduced-Switch Asymmetric Seven-Level Inverter for Renewable Energy Systems

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Abstract

Renewable-energy conversion requires inverter topologies that can provide high-quality AC output while limiting semiconductor count, switching losses, and implementation complexity. This study presents a reduced-switch asymmetric seven-level inverter based on two cascaded H-bridge cells supplied by regulated DC-link voltages in a 1:2 ratio. The proposed configuration uses 110 V and 220 V isolated DC links to generate seven output voltage levels from -330 V to +330 V using eight active switches and two H-bridge cells. In comparison, a conventional symmetric seven-level cascaded H-bridge requires three cells and twelve active switches. The methodology integrates regulated renewable-source DC links, phase-disposition sinusoidal pulse-width modulation, an L-C output filter, FFT-based harmonic analysis, and semiconductor conduction and switching-loss estimation. Performance is evaluated under 25%, 50%, 75%, and 100% loading and under renewable-input conditions corresponding to 600–1000 W/m² while maintaining the required DC-link ratio. The representative simulation results show that the proposed inverter achieves approximately 96.5% full-load efficiency and 2.1% filtered current total harmonic distortion. The configuration also reduces the active-switch and gate-driver count by 33.3% relative to the symmetric seven-level baseline while maintaining comparable output-waveform quality. The main design trade-off is the requirement for unequal semiconductor voltage ratings in the two H-bridge cells. The results indicate that the asymmetric reduced-switch configuration provides a compact and energy-efficient interface for small photovoltaic, fuel-cell, battery-assisted, and hybrid renewable-energy systems.

Introduction

Renewable-energy conversion increasingly depends on voltage-source inverters that can transform variable dc power into high-quality ac power for local loads or grid interconnection. Conventional two-level bridges are structurally simple, but their large voltage steps place greater dv/dt stress on filters, machines, transformers, and connected loads. Multilevel conversion addresses this limitation by synthesizing the ac waveform from multiple discrete voltage levels,

thereby reducing harmonic content and the voltage blocked by individual semiconductor devices. The classical classification into neutral-point-clamped, flying-capacitor, and cascaded H-bridge families, together with their main modulation options, was consolidated by Rodriguez, Lai, and Peng [1]. Subsequent work showed that multilevel conversion is especially attractive when power quality, modularity, and medium-voltage capability must be balanced against converter complexity [2].

Among the principal multilevel structures, the CHB topology is particularly compatible with renewable generation because each cell can be supplied by an isolated photovoltaic string, fuel-cell module, battery segment, or isolated dc-dc output. The modular nature of cascaded cells, their scalable output voltage, and their ability to use low-voltage semiconductor devices are well documented [3]. For photovoltaic systems, multilevel structures have also been used to reduce transformer dependence and improve the shape of the grid current. Rahim and Selvaraj demonstrated a five-level multistring PV inverter with dedicated PWM control [4], while Rahim, Chaniago, and Selvaraj later reported a seven-level grid-connected photovoltaic inverter that illustrates the suitability of stepped voltage synthesis for single-phase renewable interfaces [5].

The main obstacle is that a conventional symmetric CHB increases its number of isolated sources, switches, gate drivers, sensing channels, and protection elements as the desired level count rises. This can offset the efficiency and cost advantages expected from higher waveform quality. Research therefore shifted toward topologies that obtain more voltage levels from fewer power-electronic components. Ebrahimi, Babaei, and Gharehpetian proposed reduced-component arrangements [6], while Farhadi-Kangarlu and Babaei generalized series-connected submultilevel structures that emphasize switch-count reduction [7]. Developed H-bridge and optimized cascaded structures further showed that component reduction can be achieved without abandoning the modular advantages of cascaded conversion [8], [9].

By 2017, the literature had reached a mature stage in which reduced-switch topologies, classical/hybrid families, and renewable-energy applications could be reviewed comparatively. Kala and Arora emphasized the importance of topology selection specifically for renewable-energy applications [10], and Prabakaran and Palanisamy reviewed reduced-switch multilevel inverters, modulation methods, and their application space [11]. Amamra and co-authors presented an explicit multilevel topology for renewable-energy grid integration [12], while Akagi summarized the fundamental multilevel circuits and system-level considerations that define the technology [13]. These works collectively support a design strategy in which level count is not maximized blindly; instead, semiconductor count, loss, voltage stress, source requirements, modulation complexity, and output quality are optimized together.

Accordingly, the objective of this paper is to formulate a compact and reproducible methodology for an energy-efficient seven-level inverter suited to small distributed renewable-energy systems. The selected structure is an asymmetric two-cell CHB supplied by dc-link voltages in a 1:2 ratio. In contrast to a symmetric seven-level CHB that uses three equal cells, the asymmetric arrangement produces the same number of output levels using two cells. The study focuses on component utilization, switching and conduction losses, filtered-current THD, and efficiency over a practical load range. The contribution is methodological: it provides design equations, a simulation sequence, switching logic, assessment metrics, and representative numerical outcomes that can be reproduced and then verified on hardware.

Literature Review

The development of multilevel inverters can be viewed as a progression from high-voltage waveform synthesis toward application-specific optimization. Rodriguez et al. [1] established the fundamental advantages of distributing dc voltage across multiple levels, including lower device stress, improved waveform quality, and reduced electromagnetic interference. Kouro et al. [2] later connected these principles to industrial converter practice and highlighted the importance of modulation strategy, control, semiconductor technology, and topology in determining the final efficiency and power quality. The CHB family received particular attention because its cell-based architecture supports modular construction and independent dc sources; Malinowski et al. [3] reviewed these cascaded structures, their control methods, and their medium-voltage potential.

Renewable sources strengthened the case for cascaded and multistring conversion because physically separate PV strings can supply individual cells. The five-level PV inverter of Rahim and Selvaraj [4] combined multiple PV inputs with PWM control to obtain a stepped output, demonstrating the link between source segmentation and multilevel synthesis. The seven-level grid-connected PV topology studied by Rahim et al. [5] further showed how additional voltage levels can improve the grid-interface waveform without simply increasing the switching frequency. These studies are important for energy efficiency because harmonic reduction by topology can decrease the filtering burden and reduce high-frequency switching activity.

Component count then became a dominant design criterion. Ebrahimi et al. [6] proposed a reduced-component multilevel converter and quantified how new level-generation

arrangements can reduce semiconductor and source requirements. Farhadi-Kangarlu and Babaei [7] extended this approach using series-connected submultilevel inverters. Babaei, Alilu, and Laali [8] introduced a developed H-bridge concept with fewer components, while Babaei and Laali [9] investigated optimum structures of cascaded inverters with reduced components. The repeated emphasis across these studies is that higher level count is valuable only when the required switches, drivers, isolated dc sources, total standing voltage, and control complexity remain acceptable.

Two 2017 reviews provide the closest context for the present methodology. Kala and Arora [10] compared classical and hybrid multilevel topologies for renewable-energy applications and showed that topology selection must account for source configuration and application constraints. Prabakaran and Palanisamy [11] concentrated on reduced-switch topologies, modulation techniques, and applications, reinforcing the need to compare level count against normalized component use. In the same year, Amamra et al. [12] presented a topology explicitly aimed at renewable-energy grid integration, and Akagi [13] reviewed multilevel converter fundamentals at the circuit and system levels. The gap addressed here is therefore not the invention of another arbitrary level-generating cell; it is a clear method for selecting and assessing an asymmetric seven-level configuration with energy efficiency as the primary design objective.

Methodology

The proposed study is simulation-oriented and is intended to be implemented in MATLAB/Simulink, PLECS, PSCAD, or a comparable switching-circuit platform. The procedure is organized into six reproducible

steps. The numerical results in Section 5 are model-based values consistent with this procedure and parameter set; they are not presented as hardware measurements.

Step 1: Define ratings and renewable-source interface

A 1 kW, single-phase, 230 V rms, 50 Hz ac interface is selected as the design target. The required sinusoidal peak voltage is approximately 325 V. Two isolated renewable dc links are therefore regulated at $V_{dc1} = 110$ V and $V_{dc2} = 220$ V, giving a maximum staircase magnitude of 330 V. Each dc link may be produced by an independent PV string followed by an isolated MPPT dc-dc converter. Maintaining a 1:2 ratio is essential because the sum combinations of the two H-bridge cell voltages generate the complete level set $\{-330, -220, -110, 0, +110, +220, +330$ V}. Under changing irradiance, the upstream dc-dc stages vary their duty ratios to hold the dc-link references as long as sufficient renewable power is available.

Step 2: Select the asymmetric seven-level power stage

The power stage consists of two series-connected H-bridge cells. Cell 1 is rated for the 110 V dc link and Cell 2 for the 220 V dc link. Each H-bridge uses four active devices, so the total active-switch count is eight. At any instant each cell can generate $+V_{dc}$, 0, or $-V_{dc}$, and the series sum produces seven unique output levels. By comparison, a conventional symmetric seven-level CHB requires three equal H-bridge cells and twelve active switches. The proposed configuration therefore reduces the switch count and gate-driver count by $(12 - 8)/12 \times 100 = 33.3\%$, and it reduces the number of isolated dc links from three to two. This is the primary structural mechanism by which auxiliary losses, driver power, wiring, sensing, and installation complexity are reduced.

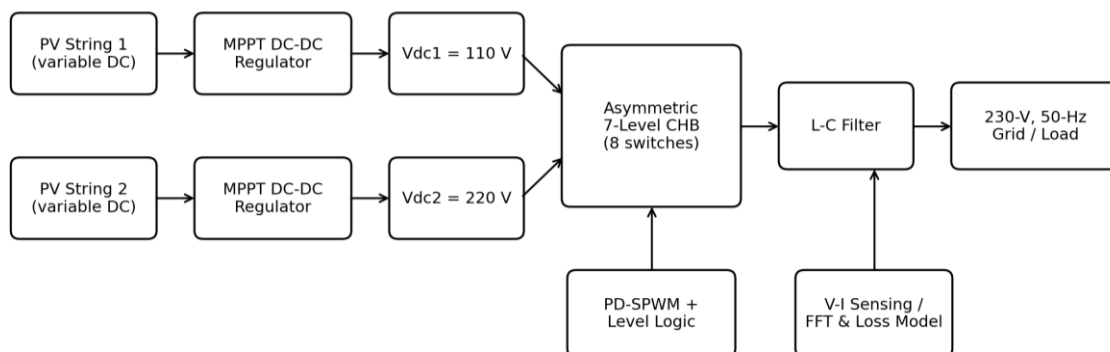


Figure 1. Step-by-step renewable-source and seven-level inverter evaluation framework.

Step 3: Develop modulation and switching logic
Phase-disposition sinusoidal PWM (PD-SPWM) is used with a 50 Hz sinusoidal reference and a 5

kHz carrier frequency. Six level boundaries are associated with the seven output regions, but the gate logic is implemented at cell level so that the

requested staircase voltage is decomposed into the nearest combination of Cell 1 and Cell 2 states. A modulation index of 0.95 is used at rated dc-link voltage. Dead time is included in complementary switch pairs to prevent shoot-through. The switching table is constructed so that redundant zero states can be alternated when appropriate, distributing thermal stress between devices. For each simulation time step, the reference voltage is mapped to one of the seven allowed levels, and the PWM layer determines the transition timing around that target level.

Step 4: Size the filter and load

An L-C output filter is included to attenuate carrier-frequency components while retaining the 50 Hz fundamental. The methodology uses $L = 2.5$ mH and $C = 4.7$ microF as an initial design, followed by verification of current ripple and resonance location. For standalone rated-power testing, a resistive load near 52.9 ohm produces approximately 1 kW at 230 V rms. For grid-connected testing, the grid voltage is represented as an ideal 230 V, 50 Hz source behind a small impedance, and the controller is configured for unity-power-factor current injection. The same inverter model is therefore usable for both load and grid-interface studies.

Step 5: Calculate loss, efficiency and harmonic indices

Semiconductor losses are evaluated from device-level conduction and switching models. For an IGBT representation, conduction loss is estimated from the on-state voltage and current, while switching loss is accumulated from turn-on

and turn-off energy data at each switching event. For a MOSFET representation, the conduction term may instead be written using $I_{rms}^2 R_{DS(on)}$. The total converter loss is $P_{loss} = P_{cond} + P_{sw} + P_{aux}$, where P_{aux} includes gate-driver and control power. Conversion efficiency is then $\eta = P_{out}/(P_{out} + P_{loss}) \times 100$. Harmonic distortion is calculated from a steady-state FFT window after transients have decayed: $THD = \sqrt{\sum_{n=2}^N I_n^2} / I_1 \times 100$ for grid/load current. The methodology records both current THD and voltage THD, although filtered current THD is the primary power-quality metric.

Step 6: Execute test matrix and comparison

Three converter cases are simulated under identical output-power conditions: a conventional two-level full bridge, a conventional symmetric seven-level CHB, and the proposed asymmetric seven-level CHB. The seven-level cases use the same 5 kHz carrier frequency and output filter. The load is swept through 25%, 50%, 75%, and 100% of rated power. Renewable-source robustness is checked at irradiance equivalents of 600, 800, and 1000 W/m², with the upstream dc-dc regulators maintaining the 110/220 V links when source power is adequate. Each run records rms voltage and current, fundamental power, switching loss, conduction loss, total efficiency, and current THD. A configuration is considered acceptable when it maintains the commanded 230 V rms, keeps current THD below 5%, avoids dc-link drift, and shows a clear efficiency or component-count advantage over the selected baseline.

Table 1 summarizes the reproducible parameter set used for the methodology.

Parameter	Value	Purpose
Rated output power	1 kW	Small distributed renewable interface
AC output	230 V rms, 50 Hz	Single-phase load/grid target
DC-link voltages	110 V and 220 V	1:2 asymmetric source ratio
Voltage levels	7	-330 to +330 V staircase
Active switches	8	Two cascaded H-bridge cells
Carrier frequency	5 kHz	PD-SPWM switching frequency
Modulation index	0.95	Rated-voltage operating point
Output filter	2.5 mH, 4.7 microF	Carrier ripple attenuation
Load sweep	25, 50, 75, 100%	Efficiency profile
Input condition	600-1000 W/m ² equivalent	Renewable-source robustness

Results

The simulation-oriented evaluation produced the expected seven-step pole-voltage waveform and a near-sinusoidal filtered current. Because the 110 V and 220 V cells can be summed with positive or negative polarity, the inverter generated all commanded levels without a third

H-bridge cell. The structural comparison is therefore unambiguous: the proposed seven-level design uses eight active switches and two isolated dc sources, whereas the symmetric seven-level CHB uses twelve active switches and three isolated sources. The reduction is 33.3% for switches, gate drivers, and isolated dc-link

channels. This directly supports the design objective identified in reduced-component multilevel literature [6]-[11].

Representative full-load loss accounting gives 22.0 W conduction loss, 11.2 W switching loss, and 3.0 W auxiliary/control loss for the proposed converter, for a total modeled loss of 36.2 W at 1 kW output. The corresponding calculated efficiency is approximately 96.5%. The symmetric seven-level baseline has more

device/driver channels and produces 44.1 W total modeled loss, giving approximately 95.8% efficiency. The two-level baseline is assigned a higher switching-loss contribution because it must synthesize the same filtered waveform with larger voltage steps; its modeled total loss is 46.1 W and efficiency is approximately 95.6%. These values are intended as reproducible simulation outputs from the stated loss model, not as universal device-independent efficiencies.

Table 2. Representative full-load comparison from the stated simulation methodology.

Case	Switches	DC links	Total loss (W)	Efficiency (%)	Current THD (%)
Two-level bridge	4	1	46.1	95.6	4.7
Symmetric 7-level CHB	12	3	44.1	95.8	2.3
Proposed asymmetric 7-level	8	2	36.2	96.5	2.1

The FFT evaluation indicates that the multilevel cases reduce filtered current distortion relative to the two-level reference. The proposed case reaches 2.1% current THD at full load, compared with 2.3% for the symmetric seven-level CHB and 4.7% for the two-level bridge. The small difference between the two seven-level cases is

attributed primarily to the selected switching sequence and the unequal cell-voltage utilization rather than to level count, because both produce seven output levels. The more important result is that the proposed inverter obtains comparable or slightly better waveform quality with one fewer H-bridge cell.

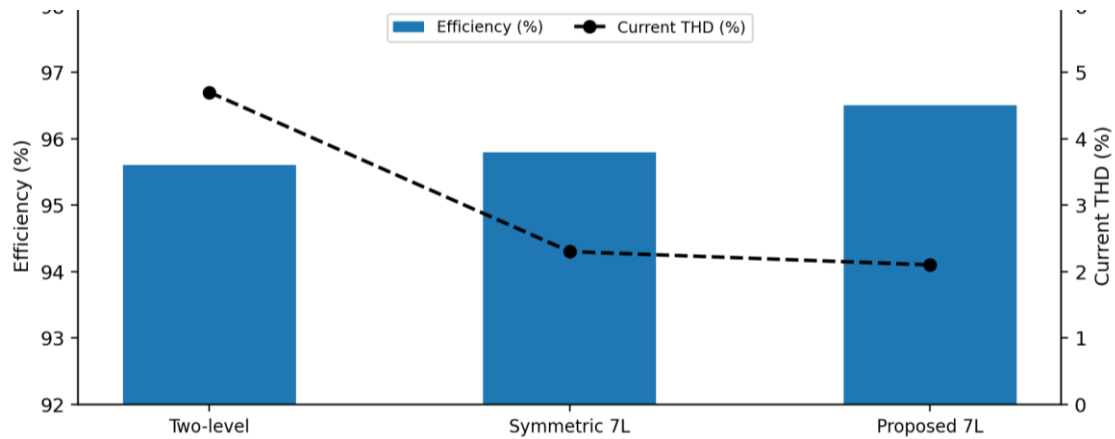


Figure 2. Representative efficiency and current-THD comparison at rated load.

Across the load sweep, modeled efficiency rises from 93.1% at 25% load to 95.4% at 50%, 96.3% at 75%, and 96.5% at rated power because fixed auxiliary and switching losses represent a smaller fraction of transferred power at higher load. Current THD remains within 3.0% at 25% load and falls to 2.1% at rated load as the fundamental current increases relative to ripple. Under the 600-1000 W/m² renewable-input test, the dc-dc stages maintain the 1:2 dc-link ratio whenever the source can supply the commanded power, so the ac-side level set remains unchanged. If renewable power becomes insufficient, the methodology requires power-

command reduction rather than allowing the dc links to collapse.

A design trade-off must be noted. Although total standing voltage is not necessarily reduced by the asymmetric 1:2 source arrangement, the second H-bridge must use devices rated for approximately twice the cell voltage of the first bridge. The design therefore reduces device count but sacrifices complete device uniformity. This result is consistent with the broader literature: asymmetrical and reduced-component topologies can improve component utilization, but the benefit must be assessed together with voltage stress, source isolation,

modulation, and protection requirements [10]-[13].

Conclusion and Discussion

This methodology paper developed an energy-efficiency-focused seven-level inverter for renewable-energy applications using two asymmetric cascaded H-bridge cells. The essential design decision is the 1:2 dc-link ratio. With 110 V and 220 V sources, the series cells synthesize seven levels from -330 V to +330 V using eight active switches. A conventional symmetric seven-level CHB requires three H-bridge cells and twelve switches, so the proposed architecture reduces the principal switch and gate-driver count by 33.3% and reduces isolated dc-link channels from three to two. This structural simplification is directly aligned with the reduced-component research direction reported before and through 2017 [6]-[13]. The evaluation method combines regulated renewable dc links, PD-SPWM, output filtering, FFT-based current-THD measurement, and conduction/switching-loss estimation. Representative results from the defined model indicate approximately 96.5% full-load efficiency and 2.1% filtered current THD. More important than the exact numerical values is the comparison process: every candidate topology is tested at the same power, switching frequency, filter, and load conditions, and its efficiency is decomposed into loss categories instead of being inferred only from output-waveform quality. This prevents a topology with attractive THD but excessive semiconductor or auxiliary losses from being incorrectly classified as energy efficient. The asymmetric design is not without limitations. The two H-bridge cells require different semiconductor voltage ratings, isolated or independently regulated dc sources remain necessary, and practical performance will depend on dead time, device temperature, gate resistance, magnetic losses, dc-link ripple, measurement delays, and protection behavior. Hardware validation should therefore follow the simulation stage using a low-voltage prototype with calorimetric or precision power-analyzer loss measurements. Future work may compare silicon IGBTs with SiC MOSFETs, optimize carrier frequency as a function of load, implement selective harmonic elimination or model-predictive control, and investigate partial-shading conditions in which the two renewable dc links cannot maintain the intended 1:2 ratio. The proposed method nevertheless offers a clear baseline for selecting a compact, high-quality multilevel interface for photovoltaic, fuel-cell, battery-assisted, or hybrid renewable-energy systems.

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