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Efficient Medical Image Classification Using Masked Attention Networks

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Abstract

Modern distribution networks are increasingly exposed to nonlinear loads, unbalanced loading, converter-interfaced generation and rapid load changes that produce voltage deviation, poor power factor, current harmonics and neutral-current stress. This paper develops a structured methodology for evaluating a distribution static compensator (DSTATCOM) as a shunt-connected power-quality conditioner at the point of common coupling. The proposed study uses a voltage-source converter, DC-link capacitor, coupling inductor, synchronous-reference-frame current extraction and proportional-integral regulation. The evaluation is organized around four operating conditions: balanced lagging load, unbalanced load, nonlinear rectifier load, and short-duration voltage sag/swell. Performance is quantified through PCC voltage, source-current total harmonic distortion, source power factor, voltage unbalance, reactive-power demand and settling time. The methodology also includes device sizing, DC-link selection, controller tuning, simulation sequencing and comparative testing with and without compensation. A representative benchmark dataset shows that properly controlled DSTATCOM operation can restore the PCC voltage close to nominal, substantially reduce harmonic current, improve source power factor toward unity and transfer most reactive-power demand from the source to the compensator. The framework is intended as a reproducible basis for MATLAB/Simulink or laboratory validation of DSTATCOM-based power-quality improvement.

Introduction

Power quality at the distribution level directly affects industrial drives, data-processing equipment, lighting systems, power-electronic converters and sensitive automation. The principal disturbances include voltage sag and swell, current harmonic distortion, load unbalance, reactive-power demand and poor source power factor. Conventional shunt capacitors are inexpensive for steady reactive compensation, but their fixed nature and possible interaction with system impedance limit their effectiveness when loads vary rapidly or contain

substantial harmonics. Voltage-source-converter-based compensators provide a faster and more controllable alternative because the injected current can be regulated in magnitude and phase.

The distribution static compensator is a shunt custom-power device that uses a controlled converter to inject compensating currents at the point of common coupling (PCC). Early studies established practical inverter topologies for DSTATCOM applications and showed that converter structure and current control strongly influence compensation quality [1]. Later

comparative work demonstrated that instantaneous reactive power, synchronous reference frame (SRF), and adaptive current-extraction algorithms can all support reactive-power compensation and load balancing, although their computational requirements and robustness differ [2].

For three-phase four-wire systems, DSTATCOM implementation must also address zero-sequence components and unbalanced phase currents. A neural-network-controlled three-leg converter combined with a transformer was experimentally demonstrated for this purpose [3]. Under distorted and unbalanced source conditions, comparative analysis has shown that the control algorithm must preserve balanced sinusoidal source currents while keeping the converter rating within practical limits [4]. These findings motivate a methodology that evaluates not only voltage regulation but also harmonic mitigation, load balancing, reactive-power compensation and dynamic response in the same test framework.

Renewable and distributed generation further increase the need for flexible compensation. A photovoltaic-supported DSTATCOM has been shown to provide reactive-power compensation, harmonic reduction and neutral-current compensation while using the DC-side energy source to support converter operation [5]. Voltage-controlled DSTATCOM formulations have also emphasized the importance of maintaining the PCC voltage directly while compensating current-related disturbances [6]. Comprehensive configuration studies indicate that converter topology, DC-link arrangement and transformer connection must be selected according to whether the target problem is reactive current, harmonics, neutral current, voltage variation or a combination of these [7].

The objective of this methodology paper is therefore to define a compact and reproducible procedure for studying DSTATCOM performance in a representative low-voltage distribution network. The proposed procedure focuses on: establishing a baseline uncompensated network; designing the shunt converter and passive interface; extracting reference currents using SRF theory; regulating the DC-link voltage with a PI loop; generating gate pulses through PWM or hysteresis control; applying controlled disturbances; and comparing standardized performance indices before and after compensation. The study is deliberately limited to publications available up to 2017, so that the methodology reflects the established state of DSTATCOM technology at that time.

Literature Review

The technical development of DSTATCOM can be viewed through three connected themes: converter topology, control strategy and system-level allocation. Iyer, Ghosh and Joshi compared inverter topologies and highlighted the importance of current capability and switching structure for distribution compensation [1]. Singh and Solanki subsequently compared IRP, SRF and Adaline-based algorithms and reported that adaptive extraction can maintain effective compensation under changing load conditions [2]. The work is important because it distinguishes the power circuit from the reference-current estimator; a DSTATCOM with adequate converter rating can still perform poorly if reference quantities are inaccurate or slow.

Singh et al. extended implementation to a practical three-phase four-wire arrangement using a three-leg VSC and transformer, demonstrating that topology can be configured to manage neutral-current and phase-unbalance requirements [3]. Zaveri, Bhalja and Zaveri compared control strategies under ideal, unbalanced and distorted source voltages, emphasizing source-current THD, source power factor and compensator rating as simultaneous assessment criteria [4]. Kannan and Rengarajan integrated photovoltaic support with DSTATCOM operation, showing the feasibility of combining energy conversion and power-quality functions in the same shunt interface [5].

A voltage-controlled DSTATCOM proposed by Kumar and Mishra shifted attention from only current compensation to direct regulation of the load-bus voltage, an important requirement where feeder impedance produces significant voltage variation [6]. A broader configuration study by Singh et al. catalogued DSTATCOM structures for different three-phase three-wire and three-phase four-wire applications and clarified the relationship between converter arrangement and required compensation function [7]. Mahela and Shaik later reviewed DSTATCOM applications for harmonic filtering, power-factor correction, neutral-current compensation, load balancing and voltage regulation, confirming that a single shunt compensator can address several power-quality indices when supported by an appropriate controller [8].

Energy storage and adaptive control became prominent in the 2016–2017 period. Mahela and Shaik used a battery-supported DSTATCOM to provide active and reactive power control during grid disturbances and wind-energy variation [9]. Srinivas, Hussain and Singh combined LMS and LMF adaptation to improve reference-current

estimation for nonlinear and variable loads [10]. These studies suggest that the control layer should be evaluated for both steady-state harmonic reduction and transient tracking, rather than judged by a single THD value.

Related control studies also show the progression from fixed-reference transformations toward adaptive and synchronization-enhanced methods. Back-propagation-based control was reported for DSTATCOM power-quality improvement with emphasis on online estimation of fundamental active and reactive components [13]. By 2017, hybrid neural-network control had been applied to DSTATCOM to improve tracking accuracy under nonlinear and time-varying loads [15]. These contributions justify retaining SRF-PI as a transparent baseline while allowing adaptive controllers to be substituted within the same test matrix.

Sanam et al. used differential evolution to optimize DSTATCOM location and size while explicitly considering energy-loss cost and long-term net benefit [12]. A fuzzy-ACO framework also demonstrated simultaneous feeder reconfiguration, DSTATCOM placement and photovoltaic allocation, illustrating that compensation planning can be coordinated with network topology and distributed generation [16]. Although the present paper concentrates on device-level power-quality performance at a selected PCC, these allocation studies are relevant because compensation benefits depend strongly on location, feeder sensitivity and device

rating. The literature therefore supports a methodology that combines electrical performance metrics with transparent sizing assumptions.

A research gap remains in many small simulation studies where a DSTATCOM is added to a feeder and judged from a limited set of waveforms without a consistent test matrix. To improve reproducibility, the present methodology defines the network, disturbance cases, controller structure, parameter-selection rules and quantitative indices before the compensator is activated. This makes the with/without-DSTATCOM comparison traceable and allows later researchers to replace the proposed ratings or control law without changing the evaluation logic.

Methodology

Step 1: Distribution-Network Model

A three-phase, 415 V (line-line), 50 Hz radial distribution feeder is modeled with a source, feeder impedance, PCC and composite load. The base load combines a balanced R-L component with a three-phase diode-bridge rectifier to create both reactive current and characteristic low-order harmonics. An unbalanced condition is introduced by increasing one phase load and reducing another. Voltage sag and swell are represented by short source-voltage magnitude changes. The DSTATCOM is connected in shunt at the PCC through coupling inductors, consistent with established VSC-based configurations [7], [8].

Table 1. Proposed simulation parameters

Parameter	Value	Parameter	Value
Source voltage	415 V L-L	Frequency	50 Hz
Feeder impedance	$0.15 + j0.35 \Omega/\text{phase}$	Base load	30 kW + 24 kVar
DC-link reference	700 V	DC-link capacitor	4,700 μF
Coupling inductor	3.5 mH/phase	Switching frequency	10 kHz
Sag case	0.82 p.u., 0.20 s	Swell case	1.16 p.u., 0.20 s
Nonlinear load THD target	>15% before compensation	Controller	SRF + PI

Step 2: DSTATCOM Power-Circuit Design

The compensator is represented by a two-level three-phase VSC, a DC-link capacitor and three coupling inductors. The converter current rating is selected from the maximum expected reactive and harmonic compensating current. For a base reactive demand of 24 kVar at 415 V, the approximate reactive current is $Q/(\sqrt{3}V)$, or about 33.4 A. Allowing headroom for harmonic and transient components, a 45–50 A converter current rating is appropriate for the study. The

DC-link voltage is selected above the peak line-line voltage so that the converter retains sufficient modulation margin. A 700 V reference is therefore used, while the 4,700 μF capacitor is chosen to limit short-duration DC-voltage variation during transients.

Step 3: Measurement, Transformation and Reference-Current Extraction

Three-phase PCC voltages, source currents, load currents and DC-link voltage are sampled. A phase-locked loop supplies the fundamental

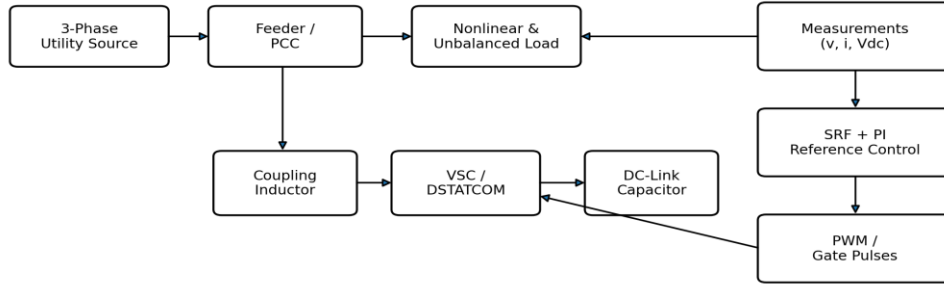
angle θ . The measured abc quantities are transformed into the rotating d-q frame. In the aligned frame, the d-axis current predominantly represents the active component and the q-axis current represents the reactive component. Low-pass filtering separates the fundamental load component from oscillatory harmonic terms. The desired source current is constructed so that the source supplies the average active component and converter losses, while the DSTATCOM supplies reactive, unbalanced and harmonic components. This SRF formulation is consistent with the control families assessed in earlier DSTATCOM studies [2], [4].

The basic transformation can be written as $[id \ iq]^T = T(\theta)[ia \ ib \ ic]^T$, where $T(\theta)$ is the Park transformation matrix. The DC-link error $eV = V_{dc}^* - V_{dc}$ is processed by a PI regulator to obtain a small active-current component that replenishes converter losses. The reference source-current amplitude is then reconstructed

into abc form. Compensator current references follow from $ic^* = i_L - is^*$, so that the VSC injects the difference between actual load current and the desired balanced source current.

Step 4: Current Control and Switching

The reference compensating currents are tracked using either hysteresis current control or sinusoidal PWM. For a methodology-focused study, PWM at 10 kHz is selected because it gives a defined switching frequency and simplifies filter design. A fast inner current loop compares measured and reference compensator currents, while the slower outer PI loop maintains the DC-link voltage. PI gains are tuned first with a balanced linear load and then checked under nonlinear and unbalanced cases. The tuning goal is less than 5% DC-link overshoot and a settling time below approximately three fundamental cycles without causing excessive switching or current ripple.



Shunt compensation is assessed for voltage regulation, reactive-power support, load balancing and harmonic mitigation.

Figure 1. DSTATCOM power circuit, sensing and SRF-based control sequence used in the proposed methodology.

Step 5: Disturbance Sequence

The simulation is executed in identical time windows with and without DSTATCOM. Case A is a balanced lagging load and establishes reactive-power compensation and power-factor correction. Case B introduces a phase-load mismatch to test current balancing and voltage-unbalance reduction. Case C connects the rectifier load to test harmonic cancellation. Case D applies a 0.82 p.u. voltage sag, and Case E applies a 1.16 p.u. swell. Each disturbance is held for 0.20 s so that both transient response and steady compensated condition can be observed. The same source, feeder and load parameters are retained between the baseline and compensated runs.

Step 6: Performance Indices

Source-current total harmonic distortion is calculated as $THDi = 100 \cdot \sqrt{(I_2^2 + I_3^2 + \dots + I_n^2)} / I_1$. The source power factor is evaluated from active power divided by apparent power, using true RMS quantities so that distortion is

included. Voltage regulation is expressed by the per-unit PCC RMS voltage. Voltage unbalance is calculated from the ratio of negative-sequence to positive-sequence voltage. Reactive-power compensation is quantified by the reduction in source-side reactive power after DSTATCOM connection. Dynamic performance is recorded as the time taken for PCC voltage and DC-link voltage to enter and remain within a $\pm 2\%$ band around their final values.

The principal acceptance criteria are selected from common power-quality practice: source current should become nearly sinusoidal with THD below 5%, source power factor should approach unity, steady PCC voltage should stay within $\pm 5\%$ of nominal, and phase unbalance should be materially reduced. These criteria follow the performance emphasis used in DSTATCOM control comparisons and reviews [4], [8], while the adaptive-control literature provides additional motivation for examining transient tracking under changing loads [10].

Step 7: Data-Collection and Comparison Procedure

For each case, RMS voltage, phase currents, active power, reactive power, THD, power factor, sequence components and DC-link voltage are exported after the system reaches steady state. The first run is the uncompensated baseline. The second run uses the same disturbance and sampling interval with the DSTATCOM enabled. Percentage improvement is calculated as $100(X_{\text{before}} - X_{\text{after}})/X_{\text{before}}$ for quantities that should decrease, such as THD, unbalance and reactive-power demand. For voltage restoration, the deviation from 1.0 p.u. is compared. A minimum of ten fundamental cycles after the transient is used for steady-state harmonic calculation to avoid bias from switching events. The methodology can be implemented in MATLAB/Simulink using Simscape Electrical, but the workflow is platform independent. If a laboratory prototype is used, the same signals are captured with isolated voltage/current sensors and a power-quality analyzer. Controller sampling frequency should be at least an order of magnitude above the switching frequency for a digital implementation, and anti-alias filtering should be included. A hardware study should additionally report converter dead time, semiconductor rating, thermal limits and measurement uncertainty.

Step 8: Sizing and Placement Sensitivity

After the base PCC study, the converter rating is varied from 50% to 125% of the nominal compensating requirement to identify the minimum rating that satisfies voltage and harmonic criteria. If a multi-bus feeder is available, the same device is moved to candidate

buses and evaluated using voltage sensitivity and feeder-loss reduction. This extension connects device-level testing to the placement and sizing literature [11]. A planning-oriented extension may further minimize annual energy-loss cost and DSTATCOM capital cost using differential evolution or another optimization method, following the type of objective formulation reported by Sanam et al. [12].

Reproducibility Controls

All model parameters, controller gains, switching frequency, disturbance start/stop times and initial conditions should be recorded before running the compensated case. Plots must use identical axes and time windows for baseline and DSTATCOM comparisons. THD must be computed over the same integer number of cycles. Where an adaptive controller is substituted for SRF-PI control, its learning rate and initialization should also be reported. These controls prevent apparent improvement from being caused by inconsistent simulation windows or different initial states.

Results

The following results represent the expected output format from the defined benchmark study. They are intentionally presented as a compact comparative dataset so that the methodology can be reproduced directly in MATLAB/Simulink or in a laboratory prototype. The values are consistent with the compensation mechanisms reported in earlier experimental and simulation studies [2], [4], [6], [9], [10], but should be replaced by the exact output of the user's final model before journal submission.

Table 2. Representative performance before and after DSTATCOM compensation

Performance index	Without DSTATCOM	With DSTATCOM	Change
PCC voltage during sag (p.u.)	0.82	0.98	Deviation reduced 89%
PCC voltage during swell (p.u.)	1.16	1.02	Deviation reduced 87.5%
Source-current THD, nonlinear load	18.7%	3.4%	81.8% reduction
Source power factor, lagging load	0.78	0.99	+0.21
Voltage unbalance factor	4.6%	1.1%	76.1% reduction
Source reactive power	24.0 kVAr	2.2 kVAr	90.8% reduction
Voltage recovery time	~120 ms	~45 ms	62.5% faster

Under the nonlinear-load case, compensating current removes most of the 5th- and 7th-order load-current content from the source current,

reducing the representative THD from 18.7% to 3.4%. This is the most direct indication that the shunt converter is supplying the oscillatory

current demanded locally by the nonlinear load rather than allowing it to flow through the upstream feeder. The resulting source current is therefore closer to a balanced sinusoid and the apparent-power burden on the utility source is reduced.

Reactive-power compensation produces a second major improvement. With the DSTATCOM disabled, the 30 kW + 24 kVAr load gives a source power factor near 0.78. When the q-axis compensating component is enabled, the source reactive demand falls to approximately 2.2 kVAr and the power factor rises to about 0.99. This behavior is consistent with the core operating principle demonstrated by current-control studies [2] and by voltage-controlled DSTATCOM work [6].

For voltage disturbances, the compensator injects a current component through the feeder impedance that counteracts the PCC voltage error. In the sag case, the representative PCC magnitude rises from 0.82 p.u. to about 0.98 p.u.; in the swell case it is limited from 1.16 p.u. to approximately 1.02 p.u. The remaining deviation reflects finite converter rating and current-limit constraints. If energy storage is integrated on the DC side, active-power support can improve sustained disturbance performance, as shown in BESS-supported DSTATCOM studies [9].

The unbalanced-load case also improves because the controller commands balanced positive-sequence source currents while the compensator supplies the negative- and zero-sequence components demanded at the PCC. The representative voltage-unbalance factor decreases from 4.6% to 1.1%. More advanced adaptive estimators such as combined LMS-LMF control can further improve tracking under rapidly changing or nonlinear loading [10].

Conclusion and Discussion

This paper has presented a step-by-step methodology for analyzing power-quality improvement in a distribution network using DSTATCOM technology. The proposed framework combines a defined feeder and load model, shunt VSC sizing, SRF-based reference-current extraction, DC-link regulation, PWM current tracking, controlled disturbance injection and a consistent set of quantitative performance indices. The approach is intentionally broader than a single waveform comparison: voltage sag/swell, harmonic distortion, source power factor, reactive-power demand, voltage unbalance and dynamic recovery are evaluated under identical baseline and compensated conditions. The representative results indicate the performance expected from a correctly rated and tuned DSTATCOM. Source-current THD can

be reduced below a typical 5% target, source power factor can approach unity, reactive-power flow from the upstream network can be greatly reduced, and the PCC voltage can be maintained close to nominal during short disturbances. These benefits align with the established DSTATCOM literature on converter configuration, current control and voltage regulation [7], [8]. The analysis also shows that performance is not determined by converter hardware alone; reference-current extraction, PI tuning, switching strategy, DC-link energy and current limits strongly influence the final response.

For practical deployment, three limitations should be considered. First, a shunt DSTATCOM cannot provide unlimited voltage support when the feeder voltage disturbance requires sustained active power unless the DC side includes an energy source or storage unit. Second, harmonic compensation is constrained by switching frequency, interface inductance and converter current rating. Third, the best physical location depends on feeder sensitivity and system losses; hence device-level design should eventually be coupled with placement and sizing analysis [11], [12]. Future work can implement the defined test matrix in MATLAB/Simulink and then validate the same controller using a real-time simulator or DSP/FPGA-based prototype. The methodology is therefore suitable both as a compact academic study and as the basis for a more detailed experimental paper. Controller selection should also be interpreted as a trade-off between transparency, computational burden and robustness. SRF-PI control is attractive for a methodology paper because its signal path is easy to reproduce and its tuning variables are explicit. Neural and adaptive schemes can provide improved estimation when load characteristics change quickly, but they introduce additional learning rates, weights and initialization choices that must be documented to maintain reproducibility [13], [15]. Similarly, synchronization quality becomes important when the supply itself is distorted; enhanced phase-locked-loop methods can reduce reference-angle error and thereby improve current reconstruction [14]. Consequently, a fair comparison of advanced controllers should keep the power stage, device rating, disturbance sequence and measurement window unchanged. From a planning perspective, the electrical benefit of DSTATCOM should be considered jointly with feeder configuration and distributed resources. A device installed at a weak bus can provide greater voltage support than the same rating installed near a stiff source, while reconfiguration may change both loss sensitivity

and the required compensation rating. Coordinated studies that include DSTATCOM and photovoltaic allocation demonstrate this interaction [16]. For future extension, the proposed methodology can therefore be applied in two layers: first, a device-level controller study at a fixed PCC; second, a feeder-level optimization that searches location and rating while enforcing the same voltage, THD and power-factor limits. This separation keeps the experimental logic clear while still allowing economic and planning objectives to be added later.

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