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Energy-Efficient Multilevel Inverter Topologies for Renewable Energy Applications

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Abstract

Multilevel inverters (MLIs) are attractive interfaces for photovoltaic, wind, fuel-cell, and energy-storage systems because they synthesize a near-sinusoidal AC waveform from multiple DC voltage levels while reducing device voltage stress and filtering demand. This methodology paper develops a reproducible framework for selecting an energy-efficient MLI topology using literature available up to 2015. The framework compares neutral-point-clamped (NPC), flying-capacitor (FC), cascaded H-bridge (CHB), and reduced-switch cascaded structures on semiconductor count, auxiliary components, DC-source requirements, switching/conduction loss tendency, harmonic quality, voltage stress, control burden, and renewable-source compatibility. A common 9-level, single-phase design basis is used for analytical comparison, while a normalized selection index prevents any one metric from dominating the decision. The study shows why CHB structures are naturally suited to modular renewable DC sources, whereas reduced-switch cascaded topologies can further improve device economy and lower gate-drive and switching-loss burden. The proposed method is intended as a practical pre-simulation screening procedure before detailed MATLAB/Simulink or hardware validation.

Introduction

Renewable-energy systems deliver electrical power from sources whose voltage magnitude and operating point vary with irradiance, temperature, wind speed, state of charge, and loading. The inverter therefore has to perform more than simple DC-to-AC conversion: it must provide acceptable voltage quality, low semiconductor losses, manageable device stress, and a structure that can be scaled without excessive filters or magnetic components. The neutral-point-clamped converter introduced by Nabae, Takahashi, and Akagi established the practical three-level voltage-source inverter concept and demonstrated the value of dividing the DC-link voltage among semiconductor devices [1]. Lai and Peng subsequently organized

the principal multilevel families—diode-clamped, capacitor-clamped, and cascaded inverters—and emphasized their ability to synthesize staircase voltage waveforms for high-power conversion [2].

Compared with a two-level inverter, increasing the number of output voltage levels reduces the voltage step applied to the load and can lower harmonic content for a given effective switching effort. Tolbert, Peng, and Habetler showed that multilevel conversion permits near-sinusoidal voltages with low switching frequency and is compatible with multiple isolated DC sources [3]. The broad survey by Rodríguez, Lai, and Peng confirmed that device voltage stress, harmonic performance, and topology-dependent balancing requirements are the key trade-offs when

selecting an MLI [4]. For renewable generation, this trade-off is especially important because photovoltaic strings, isolated DC/DC modules, batteries, or rectified wind-generator outputs can provide naturally segmented DC sources.

Energy efficiency in this paper is treated as a system-level property rather than only a peak conversion-efficiency number. A topology is considered energy-efficient when it can achieve the required voltage level and power quality using a small number of actively switching devices, short current-conduction paths, moderate blocking-voltage stress, limited balancing circuitry, and a modulation strategy that avoids unnecessary switching. This interpretation is consistent with the industrial review of multilevel converters by Franquelo et al., which links multilevel structures with improved waveform quality and reduced stress at higher power ratings [5]. The objective is therefore to formulate a step-by-step methodology that screens classical and reduced-device topologies using common metrics and identifies the most suitable architecture for renewable-energy applications without relying on references published after 2015.

Literature Review

Classical MLI development began with the NPC concept [1] and the broader three-family classification of Lai and Peng [2]. In an m -level diode-clamped leg, the semiconductor switch count increases approximately with $2(m-1)$, while the number of clamping diodes grows quickly with level count. This feature is acceptable for three-level industrial drives but becomes a complexity penalty as the number of levels rises. Flying-capacitor structures replace clamping diodes with capacitor networks and provide redundant switching states, but the stored-energy components and capacitor-voltage balancing effort become significant. CHB structures instead series-connect H-bridge cells, each supplied by a DC source, making them modular and attractive where multiple renewable DC sources are already available [3], [4].

Franquelo et al. described the transition of multilevel converters from research prototypes to practical high-power applications, highlighting their reduced dv/dt and improved spectral characteristics [5]. For stand-alone photovoltaic systems, Daher, Schmid, and Antunes compared multilevel inverter options and demonstrated the relevance of topology choice to PV power conditioning [6]. Their work is particularly important for renewable systems because it connects the general MLI advantages to a source

whose available DC voltage is modular and variable.

A second research direction focused on reducing the number of power devices. Babaei proposed a cascaded converter topology intended to obtain more output levels with fewer switches than conventional cascaded arrangements [7]. Babaei and Hosseini further developed a cascaded structure with a minimum-switch objective and reported reduced component requirements relative to conventional alternatives [8]. These studies established device count as a meaningful design variable because each additional semiconductor adds conduction loss, switching loss, gate-driver power, cooling demand, cost, and reliability exposure.

By 2010, cascaded multilevel inverters had become a mature research category. Malinowski et al. reviewed cascaded structures, modulation techniques, regenerative configurations, and applications, emphasizing their modularity and high output-voltage capability [9]. Kouro et al. provided a broader state-of-the-art review and identified multilevel conversion as a major technology for medium-voltage and high-power applications [10]. Abu-Rub et al. similarly summarized medium-voltage converter challenges, including device stress, reliability, modulation, and industrial implementation constraints [11]. Together, these reviews support a methodology that evaluates both electrical performance and implementation burden rather than THD alone.

Renewable-specific work also moved toward reduced-device grid interfaces. Rahim, Chaniago, and Selvaraj proposed a seven-level grid-connected inverter for photovoltaic conversion and experimentally validated a multilevel waveform suitable for PV-grid interfacing [12]. Babaei, Alilu, and Laali later proposed a developed H-bridge cascaded topology with fewer DC sources and switching components [13]. Most directly relevant to the 2015 boundary of this paper, Babaei, Laali, and Bayat presented a single-phase cascaded inverter based on a new basic unit. Their generalized structure uses $N_{\text{switch}} = 5n + 6$ and $N_{\text{source}} = 3n + 1$ for n series-connected basic units, and their experimental 15-level example used 12 unidirectional switches and seven DC sources [14]. The authors also showed that low switching frequency was selected to reduce switching losses, reinforcing the connection between device count, switching strategy, and energy efficiency [14].

The literature therefore reveals a clear progression: classical topologies established voltage sharing and waveform-quality advantages; renewable-energy studies confirmed

the usefulness of segmented DC sources; and reduced-switch research attempted to preserve multilevel benefits while lowering semiconductor and driver count. The gap addressed here is methodological: rather than

proposing another circuit, the paper defines a compact screening procedure that compares topology families on a common renewable-energy design basis before detailed simulation or prototype construction.

Table 1. Literature synthesis used to define the comparison criteria

Reference	Year	Main contribution	Methodological implication
[1] Nabae et al.	1981	NPC three-level inverter	Include clamping and DC-link balancing burden
[2] Lai & Peng	1996	Classical MLI families	Compare topology families on equal level count
[6] Daher et al.	2008	MLIs for stand-alone PV	Assess renewable-source compatibility
[7], [8] Babaei	2008–2009	Reduced-switch cascaded structures	Count switches, drivers and sources
[9], [10] Reviews	2010	Cascaded and industrial MLI state of art	Include modulation, stress and scalability
[12] Rahim et al.	2011	Seven-level PV grid inverter	Use grid-quality constraints
[13], [14] Babaei et al.	2014–2015	Developed H-bridge/basic-unit MLIs	Evaluate reduced-device candidate

Methodology

The proposed methodology is a comparative design procedure rather than a claim of new experimental hardware. All candidates are

evaluated under the same electrical assumptions so that differences are attributable to topology and switching strategy. The workflow is shown in Fig. 1.

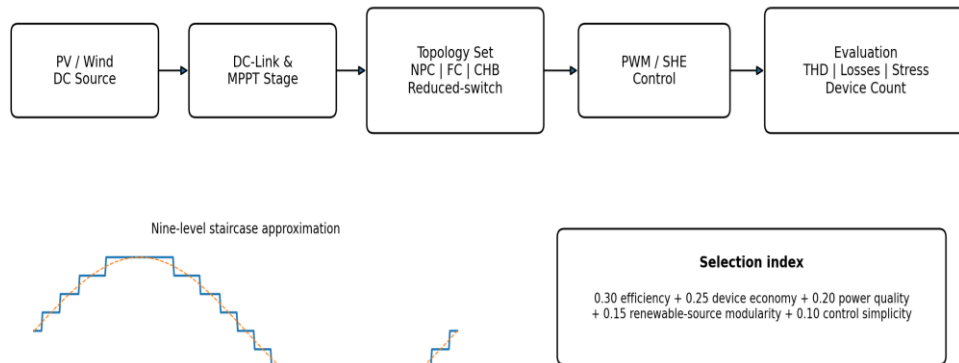


Figure 1. Original methodology workflow for topology screening and renewable-energy suitability assessment.

Step 1 — Define the renewable-energy interface
A single-phase 1 kW renewable interface is used as the reference case. The DC side represents either a PV string with MPPT/DC-link conditioning, a rectified small wind generator, a battery string, or a combination of isolated DC modules. The nominal AC output is 230 V rms at 50 Hz. A 9-level target is selected because it is high enough to reveal component-count and

balancing differences while remaining small enough for transparent analytical comparison.

Step 2 — Select topology candidates

Four candidates are screened: diode-clamped/NPC, flying-capacitor (FC), conventional cascaded H-bridge (CHB), and a reduced-switch cascaded family represented by the developed basic-unit approach in [13], [14]. The classical candidates are included because they form the accepted reference set [2], [4]; the

reduced-switch candidate is included because device reduction directly addresses switching loss, driver consumption, heat-sink loading, and converter volume.

Step 3 — Use a common modulation basis

For the screening stage, phase-disposition sinusoidal PWM is assumed for NPC and FC structures, phase-shifted carrier PWM for CHB, and low-frequency stepped or selective-harmonic operation for the reduced-switch candidate. This does not imply that one modulation is universally superior. The purpose is to pair each topology with a well-established strategy that reflects its practical use. Low switching-frequency operation is specifically important to the reduced-switch family because [14] identifies reduced switching losses as a motivation for fundamental-frequency control.

Step 4 — Calculate structural metrics

For an m -level phase leg, the classical switch-count relation $2(m-1)$ is used for NPC and FC candidates. The clamping-diode requirement for an m -level NPC phase is $(m-1)(m-2)$, and the flying-capacitor count is $(m-1)(m-2)/2$, excluding the main DC-link capacitors. For a symmetric CHB inverter, $s = (m-1)/2$ H-bridge cells are required and the active-switch count is $4s$. The developed reduced-switch family is evaluated using the published relations in [14], $N_{\text{switch}} = 5n + 6$ and $N_{\text{source}} = 3n + 1$, together with its experimentally demonstrated reduction in switches and drivers relative to several cascaded alternatives.

Step 5 — Estimate energy-loss tendency

Detailed semiconductor loss values depend on the selected IGBT/MOSFET, junction temperature, current waveform, dead time, and gate resistance. To avoid inventing device-specific efficiency values, the methodology uses two transparent loss proxies. The conduction-

path index is the average number of semiconductor devices simultaneously carrying load current, and the switching-effort index is proportional to the number of actively commutated devices multiplied by switching frequency. A lower value indicates a lower first-order loss tendency. When a detailed model is available, the proxy is replaced by $P_{\text{cond}} = \Sigma[V_{\text{CE0}} \cdot I_{\text{avg}} + r_{\text{CE}} \cdot I_{\text{rms}}^2]$ and $P_{\text{sw}} = \Sigma f_{\text{sw}}(E_{\text{on}} + E_{\text{off}})$, and converter efficiency is $\eta = P_{\text{out}} / (P_{\text{out}} + P_{\text{cond}} + P_{\text{sw}} + P_{\text{aux}})$.

Step 6 — Evaluate waveform quality and device stress

Output-voltage total harmonic distortion is calculated as $\text{THD} = \sqrt{\Sigma V_h^2} / V_1$ for harmonics $h \geq 2$. The topology is also checked for maximum device blocking voltage, DC-link or flying-capacitor balancing requirements, common-mode behavior, and the need for isolated sources. A topology that achieves a low switch count but transfers excessive voltage stress to a small number of devices is not automatically considered energy-efficient, because higher-voltage devices may have larger conduction and switching losses.

Step 7 — Rank the alternatives

Each topology receives a 1–5 score for efficiency potential, device economy, power quality, renewable-source modularity, and control simplicity. The weighted selection index is $0.30(\text{Efficiency}) + 0.25(\text{Device economy}) + 0.20(\text{Power quality}) + 0.15(\text{Modularity}) + 0.10(\text{Control simplicity})$. The weights intentionally favor energy and hardware efficiency while retaining waveform quality and practical integration as decision factors. The ranking is a screening result; final design approval still requires semiconductor-level simulation and thermal verification.

Table 2. Common analytical design basis for the comparison

Parameter	Value	Parameter	Value
Rated output power	1 kW	AC output	230 V rms, 50 Hz
Target levels	9	Load basis	0.95 power factor RL
PWM range	2–10 kHz	Low-frequency case	50 Hz stepped/SHE
Quality metric	Voltage THD	Efficiency metrics	Conduction + switching proxies
Comparison set	NPC, FC, CHB	Advanced candidate	Reduced-switch cascaded

Validation and reproducibility

The analytical screening is followed by a reproducible simulation sequence. First, each topology is configured for the same nine voltage levels and fundamental output magnitude. Second, identical load and carrier conditions are

applied. Third, FFT analysis is performed over an integer number of fundamental cycles after steady state. Fourth, semiconductor currents, blocking voltages, and switching transitions are logged. Fifth, loss calculations use the same device data sheet and junction-temperature

assumption for every candidate. Finally, a sensitivity test varies the modulation index and renewable DC-source mismatch by $\pm 10\%$. This sequence prevents a topology from appearing superior simply because it was tested at a different operating point. It also separates topology-related benefits from control-related benefits, an important distinction because multilevel reviews repeatedly show that modulation and converter structure interact strongly [4], [9], [10].

Results

Applying the structural part of the methodology to a nine-level single-phase stage produces the comparison in Table 3. NPC and FC alternatives require the same number of active switches for a given level count, but they add a rapidly increasing number of clamping diodes or balancing capacitors. CHB uses the same 16-switch count at nine levels, yet avoids clamping diodes and flying capacitors; its main cost is the need for four isolated DC sources. That requirement can be a disadvantage with a single bulk DC bus but is often compatible with modular PV strings, isolated DC/DC outputs, batteries, or fuel-cell modules [3], [6], [9].

The reduced-switch cascaded family is the strongest candidate when the design objective prioritizes semiconductor economy. The 2015 developed topology uses five-switch basic units plus an output H-bridge and reports $N_{\text{switch}} = 5n + 6$ and $N_{\text{source}} = 3n + 1$ [14]. In its experimentally demonstrated 15-level configuration, two basic units and one additional

DC source produced 15 levels using 12 unidirectional switches and seven DC sources [14]. More importantly for scaling, the authors reported that a minimum 63-level realization using their fourth source-selection algorithm required 19 IGBTs, 19 power diodes, 19 driver circuits, and 10 DC sources, whereas a compared cascaded alternative required 44 of each semiconductor/driver and 11 DC sources [14]. This result supports the methodology's use of switch and driver count as energy-efficiency proxies, because fewer actively commutated devices reduce the number of loss-generating switching events and auxiliary gate-drive channels.

The weighted selection index therefore ranks conventional CHB and reduced-switch cascaded structures highest for renewable applications. CHB receives the strongest modularity score and a high power-quality score, while the reduced-switch family receives the strongest device-economy and switching-loss-potential scores. NPC remains attractive when a common DC bus and mature industrial hardware are priorities, but its clamping network becomes cumbersome at high level count. FC provides switching-state redundancy but has the lowest score in this screening because capacitor count and voltage-balancing effort add loss, volume, and control burden. These are comparative screening results rather than measured efficiency percentages; detailed converter efficiency must be obtained using the device-level validation described in Section 3.8.

Table 3. Comparative screening result for renewable-energy use

Topology	9-level active switches	Extra passive / clamping burden	DC-source structure	Loss tendency	Balancing burden	Renewable fit	Weighted score /5
NPC	16	56 clamping diodes; split DC link	Common DC bus	Medium	Medium-High	Good	3.55
Flying capacitor	16	28 flying capacitors + DC link	Common DC bus	Medium-High	High	Moderate	3.10
Conventional CHB	16	No clamping network	4 isolated sources	Low-Medium	Low	Very good	4.25

Reduced-switch cascaded	Lower than comparable cascaded designs; topology-dependent	Reduced gate-drive count; no classical clamping network	Multiple unequal/equal DC sources	Low potential with low-frequency control	Low-Medium	Very good	4.45
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The ranking is robust to moderate changes in weighting. Increasing the weight of control simplicity improves NPC slightly, while increasing modularity favors CHB. Increasing the weight of device economy favors the reduced-switch family. Thus, the method does not identify a universally best inverter; it identifies the best match between a renewable source architecture and the dominant design constraints.

Conclusion and Discussion

This paper presented a step-by-step methodology for evaluating energy-efficient multilevel inverter topologies for renewable-energy applications using only literature available through 2015. The method deliberately separates topology screening from detailed semiconductor simulation. In the first stage, the designer fixes the required voltage level, source architecture, power rating, and waveform requirements. In the second stage, candidate topologies are compared using switch count, auxiliary component count, DC-source burden, conduction path, switching effort, device stress, balancing complexity, and power-quality capability. In the final stage, the best candidates are subjected to identical device-level loss and thermal models. The literature indicates that classical NPC, FC, and CHB structures each solve different high-voltage conversion problems. NPC is well established and works naturally from a common DC link, but clamping-device count rises with voltage level [1], [2], [4]. FC provides redundant states but requires extensive capacitor management. CHB is especially compatible with renewable systems because its isolated DC cells can be associated with separate PV strings, storage modules, or isolated converters [3], [6], [9]. The principal CHB disadvantage is the number of semiconductor devices and isolated sources as the level count rises. Reduced-switch cascaded research up to 2015 directly addressed this limitation. The works of Babaei and co-authors progressively reduced power-switch, driver, and source requirements [7], [8], [13], [14]. The 2015 basic-unit topology is particularly relevant because it combines generalized level generation with low-frequency switching and experimentally demonstrated multilevel operation [14]. From an energy-efficiency perspective, fewer switches

can reduce switching-event count, gate-drive power, heat generation, and cooling demand; however, these benefits must be checked against the blocking-voltage rating and conduction path of the remaining devices. For practical renewable-energy design, the outcome of this study is therefore conditional. A conventional CHB is recommended when source modularity, straightforward cell replication, and independent DC segments are the dominant concerns. A reduced-switch cascaded topology is recommended when compactness and semiconductor economy are dominant and unequal DC-source magnitudes can be implemented reliably. NPC remains appropriate where a single high-voltage DC link and industrially mature neutral-point control are preferred. FC is most defensible where switching-state redundancy is valuable enough to justify its capacitor-balancing burden. The main limitation is that the results table is a topology-screening assessment rather than a substitute for measured efficiency. Future implementation should use the same IGBT or MOSFET data, identical thermal boundary conditions, and identical output power for all candidates. Experimental validation should report efficiency over the expected renewable operating range, THD, common-mode voltage, device temperatures, DC-link imbalance, and transient response. Within these limits, the framework offers a concise and reproducible way to select an MLI architecture before investing in detailed simulation and hardware.

References

- Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, 1981. DOI: 10.1109/TIA.1981.4503992.
- J.-S. Lai and F. Z. Peng, "Multilevel Converters—A New Breed of Power Converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509–517, 1996. DOI: 10.1109/28.502161.
- L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel Converters for Large Electric Drives," *IEEE Transactions on Industry Applications*, vol.

35, no. 1, pp. 36–44, 1999. DOI: 10.1109/28.740843.

J. Rodríguez, J.-S. Lai, and F. Z. Peng, “Multilevel Inverters: A Survey of Topologies, Controls, and Applications,” *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002. DOI: 10.1109/TIE.2002.801052.

L. G. Franquelo, J. Rodríguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, “The Age of Multilevel Converters Arrives,” *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, 2008. DOI: 10.1109/MIE.2008.923519.

S. Daher, J. Schmid, and F. L. M. Antunes, “Multilevel Inverter Topologies for Stand-Alone PV Systems,” *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, pp. 2703–2712, 2008. DOI: 10.1109/TIE.2008.922601.

E. Babaei, “A Cascade Multilevel Converter Topology With Reduced Number of Switches,” *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2657–2664, 2008. DOI: 10.1109/TPEL.2008.2005192.

E. Babaei and S. H. Hosseini, “New Cascaded Multilevel Inverter Topology With Minimum Number of Switches,” *Energy Conversion and Management*, vol. 50, no. 11, pp. 2761–2767, 2009. DOI: 10.1016/j.enconman.2009.06.032.

M. Malinowski, K. Gopakumar, J. Rodríguez, and M. A. Pérez, “A Survey on Cascaded Multilevel Inverters,” *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197–2206, 2010. DOI: 10.1109/TIE.2009.2030767.

S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodríguez, M. A. Pérez, and J. I. Leon, “Recent Advances and Industrial Applications of Multilevel Converters,” *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, 2010. DOI: 10.1109/TIE.2010.2049719.

H. Abu-Rub, J. Holtz, J. Rodríguez, and G. Baoming, “Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications,” *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, 2010. DOI: 10.1109/TIE.2010.2043039.

N. A. Rahim, K. Chaniago, and J. Selvaraj, “Single-Phase Seven-Level Grid-Connected Inverter for Photovoltaic System,” *IEEE Transactions on Industrial Electronics*, vol. 58, no. 6, pp. 2435–2443, 2011. DOI: 10.1109/TIE.2010.2064278.

E. Babaei, S. Alilu, and S. Laali, “A New General Topology for Cascaded Multilevel Inverters With Reduced Number of Components Based on Developed H-Bridge,” *IEEE Transactions on Industrial Electronics*, vol. 61, no. 8, pp. 3932–3939, 2014. DOI: 10.1109/TIE.2013.2286561.