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Output-Voltage Enhancement for A Grid-Connected Photovoltaic System Using a LUO Converter and A Nine-Level Inverter

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Abstract

This paper reports a grid-connected photovoltaic conversion chain in which a DC-DC Luo converter raises and regulates the array voltage and a nine-level inverter synthesises the AC output, with a proportional-integral regulated DC link and pulse-width modulation. This study produced quantitative results, and they are treated as the substance of the paper: a simulated boost from 250 V input to 350 V output, a grid voltage oscillating between minus 200 V and plus 200 V, and a simulated total harmonic distortion of 4.9 %. Each is verified arithmetically rather than restated. The voltage ratio is shown to be 1.40, implying a duty ratio of 0.286 for a boost-type transfer function or 0.583 for the buck-boost form the Luo topology provides, so the reported pair is self-consistent with the topology but does not by itself identify which transfer function was simulated. The distortion figure is examined against the harmonic standard rather than against a remembered five per cent, and this revision develops that examination quantitatively. Evaluating the Fourier series of an unfiltered nine-level staircase shows that the same waveform yields 4.1 % when distortion is summed to the fifteenth harmonic and 8.3 % when summed to the fiftieth, which is the range the standard actually prescribes; the reported 4.9 % therefore lies within the band a limited harmonic range would produce, and cannot be interpreted as compliant or non-compliant until the range, the presence of an output filter and the switching-angle scheme are stated. The applicable limit is also shown to depend on which quantity and which voltage class is meant, being 8 % for voltage distortion at or below 1 kV and 5 % for current total demand distortion, so the reported margin of 0.1 percentage points against a remembered five per cent is not a well-defined margin at all. The principal limitation is stated plainly: all reported values are outputs of a simulation model, no hardware measurement was recorded, and the hardware figures in the record are photographs of an oscilloscope rather than logged data. Two internal inconsistencies are reported rather than silently reconciled.

Nomenclature

Symbol	Meaning
V_{in}, V_o	Converter input and output voltage (V)
D	Converter duty ratio
L_1, L_2, C_1, C_2	Luo converter passive elements

N	Number of inverter output levels
α_k	Switching angle of the k-th level (rad)
V_g, V_{dc}	Grid voltage and DC-link voltage (V)
V_h, V_1	Amplitude of the h-th harmonic and of the fundamental (V)
h, H	Harmonic order and the highest order included in a summation
THD, TDD	Total harmonic distortion and total demand distortion (%)
PF_{dist}	Distortion power factor
m_a	Amplitude modulation index
k_p, k_i	Proportional and integral gains
f_s	Switching frequency (Hz)

Introduction

A photovoltaic array delivers a low, variable DC voltage that must be raised and regulated before it can be inverted to grid-compatible AC. Two design choices dominate the resulting power quality: the DC-DC topology, which sets the achievable gain and the ripple presented to the array, and the inverter structure, which sets the harmonic content of the AC output [1], [4].

Multilevel inverters address the second directly. By synthesising the output from several DC levels rather than two, the staircase waveform approaches a sinusoid more closely, so distortion falls and filter requirements ease, at the cost of more switches and a more complex modulation scheme [1], [2]. This paper reports a chain combining a Luo converter with a nine-level inverter for a grid-connected array.

This study differs from many undergraduate reports in that it produced quantitative results. The paper therefore concentrates on verifying those numbers, establishing what they do and do not establish, and identifying the gap between the simulated performance and the hardware that was built.

1. Problem Statement

Simulation results for multilevel photovoltaic inverters are plentiful, and reported distortion figures cluster below the commonly quoted five per cent. What is much rarer is a clear statement of which figures are simulated and which measured, and of the conditions, being modulation index, switching frequency and harmonic range, under which a distortion figure was obtained. Without those, two published distortion values cannot be compared, and neither can be checked against a standard. This paper supplies that statement for its own results, and demonstrates numerically how much the missing conditions matter.

2. Objectives

The specific objectives of the work are as follows:

- To verify arithmetically the reported conversion ratio and the duty ratios it implies under the two candidate transfer functions.
- To assess the reported distortion figure against the harmonic standard as it is actually written, rather than against a remembered five per cent.
- To quantify how much a distortion figure depends on the harmonic range over which it is summed, using the Fourier series of the waveform in question.
- To separate the simulated results from the hardware, which produced photographs rather than logged measurements.
- To identify internal inconsistencies in the record and report rather than reconcile them silently.
- To specify the validation path that would connect the model to the hardware.

3. Scope and Delimitation

The study covers the conversion and synthesis relations, the arithmetic verification of the reported simulation outputs, and the specification of the hardware measurements that were absent. It excludes any claim of measured voltage, current, distortion, efficiency or power factor for the constructed hardware, because none was recorded. It excludes any assertion of compliance with a harmonic standard, for the reasons developed in Section V-D. And it takes no position on the correctness of the simulation itself, which cannot be checked without the model's parameters.

4. Contributions

1. Arithmetic verification of the reported conversion ratio and the duty ratios it implies under the two candidate transfer functions.
2. An assessment of the 4.9 % distortion figure against the harmonic standard as written, including the computed distortion power factor and the conditions that must accompany the value.
3. A quantitative demonstration, new to this revision, that an unfiltered nine-

level staircase yields 4.1 % or 8.3 % distortion depending only on the harmonic range summed, which brackets the reported figure and shows why the range is not an optional detail.

4. A clarification, new to this revision, that the applicable limit is 8 % for voltage distortion at or below 1 kV and 5 % for current total demand distortion, so the reported margin against a remembered five per cent is not well defined.
5. A clear separation of the simulated results from the hardware, which produced photographs rather than logged measurements.
6. Identification of two internal inconsistencies in the record, reported rather than reconciled silently.

The remainder of the paper is organised as follows. Section II reviews related work and fixes the applicable limits. Section III develops the relations. Section IV describes the simulation and the hardware. Section V reports the results and their verification. Section VI discusses the findings, Section VII states the limitations, and Section VIII gives the validation path. Sections IX and X give the conclusion and the future scope.

Related Work

Rodriguez and colleagues [1] survey multilevel inverter topologies and establish the central relation used here: harmonic content falls as the number of synthesised levels rises, with the cascaded H-bridge, neutral-point-clamped and flying-capacitor families offering different trade-offs in device count and DC-source requirements. Franquelo and colleagues [2] review the maturation of these topologies in industrial practice.

On the DC-DC stage, Luo [3] developed the voltage-lift converter family, showing that the lift technique achieves high gain without the extreme duty ratios a simple boost stage requires; Erickson and Maksimovic [4] provide the general converter analysis and loss framework. For the grid interface, Kjaer and colleagues [5] review single-phase photovoltaic inverter topologies and the power-decoupling problem that governs DC-link design. Esram and Chapman [7] define tracking efficiency for the array stage.

Table 1. Representative Related Work and its Relation to This Study

Ref.	Year	Focus and scope	Method and validation	Relation to this work
[1]	2002	Multilevel inverter topologies	Survey; analysis	Level count against harmonic content
[2]	2008	Multilevel converters in industry	Review	Practical context for the nine-level stage
[3]	1999	Voltage-lift Luo converters	Analysis; experiment	The DC-DC stage adopted
[4]	2001	Converter analysis and loss	Textbook	Transfer functions of Eqs. (1) and (2)
[5]	2005	Single-phase PV inverters	Review	Grid-interface and DC-link context
[6]	2022	IEEE Std 519 harmonic control	Recommended practice	The limits the distortion figure is judged against
[7]	2007	MPPT comparison	Review	Array-stage tracking

1. What the Harmonic Standard Actually Says

The assessment in Section V-D depends on the limit being stated precisely, and the record cites only a five per cent figure without saying which limit is meant. The governing document is IEEE Std 519, of which the 2022 edition is current and supersedes the 2014 revision. Table 2 sets out the relevant structure.

Table 2. Distortion Limits from IEEE Std 519-2022

Quantity	Limit	Applicability
Voltage, total harmonic distortion	8.0 %	Systems at or below 1.0 kV, at the point of common coupling
Voltage, individual harmonic	5.0 %	Systems at or below 1.0 kV
Voltage, total harmonic distortion	5.0 %	Systems above 1.0 kV and up to 69 kV

Current, total demand distortion	5.0 %	Short-circuit to demand-current ratio below 20
Current, 3 ≤ h < 11	4.0 % of the demand current	Short-circuit to demand-current ratio below 20
Harmonic range for evaluation	up to and including h = 50	Applies throughout the current limit tables

Values are the limits published in IEEE Std 519-2022 [6]. The limits apply at the point of common coupling between utility and user, and the current limits are the user's responsibility while the voltage limits are the utility's. Note that the standard limits total demand distortion for current, referred to the maximum demand load current, whereas Eq. (5) defines total harmonic distortion, referred to the fundamental actually flowing; the two coincide only at rated demand. Nothing in this table was measured in this work.

Three points follow immediately, and they bear directly on the 4.9 % figure. The five per cent that the record recalls is the voltage distortion limit for systems above 1 kV and, separately, the current total demand distortion limit; for a low-voltage grid connection at or below 1 kV, which is what a single-phase photovoltaic inverter of this class makes, the voltage distortion limit is 8 %. Whether the reported figure is a voltage or a current distortion is not stated. And the standard prescribes evaluation up to the fiftieth harmonic, which Section V-D shows is not a formality.

System Modelling

1. Conversion Ratio

For a boost-type transfer function the ideal ratio is

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \tag{1}$$

whereas the Luo and other fourth-order buck-boost topologies give

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \tag{2}$$

Both are used in Section V-B to interpret the reported voltages. Passive element selection follows the ripple constraints

$$L \geq \frac{V_{in} D}{f_s \, \Delta I_L}, \qquad C \geq \frac{I_o D}{f_s \, \Delta V_o} \tag{3}$$

2. Multilevel Synthesis

An N-level inverter synthesises its output from N discrete voltage steps. For a staircase approximation to a sinusoid the fundamental and harmonic amplitudes follow from the switching angles,

$$V_h = \frac{4 V_{dc}}{h\pi} \sum_{k=1}^{(N-1)/2} \cos(h\alpha_k), \qquad h = 1, 3, 5, \ldots \tag{4}$$

so that with half of one less than N independent angles the same number of harmonic constraints can be imposed, either eliminating selected low-order harmonics or minimising the aggregate. Fig. 1 shows the resulting nine-level synthesis. Distortion is then

$$THD = \frac{\sqrt{\sum_{h \geq 2} V_h^2}}{V_1} \times 100\,\% \tag{5}$$

and the associated distortion power factor is

$$PF_{dist} = \frac{1}{\sqrt{1 + (THD/100)^2}} \tag{6}$$

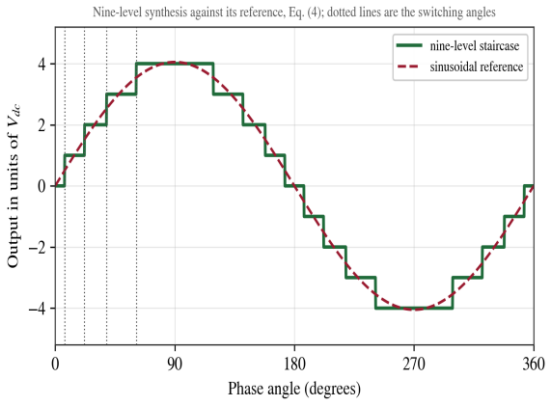

Figure 1: Nine-level staircase synthesis against its sinusoidal reference, following Eq. (4). The dotted lines mark the switching angles.

3. The Harmonic Range Is Part of the Definition

Equation (5) is written with an unbounded summation, which no measurement and no simulation can perform. Every reported distortion figure is therefore in practice

$$THD(H) = \frac{\sqrt{\sum_{h=3,5,\ldots}^{H} V_h^2}}{V_1} \times 100\,\% \tag{10}$$

for some highest order H, and two figures computed with different H are not the same quantity. This is ordinarily a minor technicality; Section V-D shows that for the waveform in question it is not.

4. DC-Link Regulation

The regulator acts on the DC-link error,

$$u = k_p e + k_i \int e \, dt, \qquad e = V^{*} - V_{dc} \tag{7}$$

setting the modulation index so that the inverter exports the array power while holding the link within its ripple band.

Simulation and Hardware

1. The Conversion Chain

Fig. 2 shows the chain as modelled: array, Luo converter with pulse-width modulation,

proportional-integral regulated DC link, nine-level inverter and grid interface. Waveforms were captured for the converter input and output, the grid current and voltage, and the harmonic spectrum from which distortion was computed.

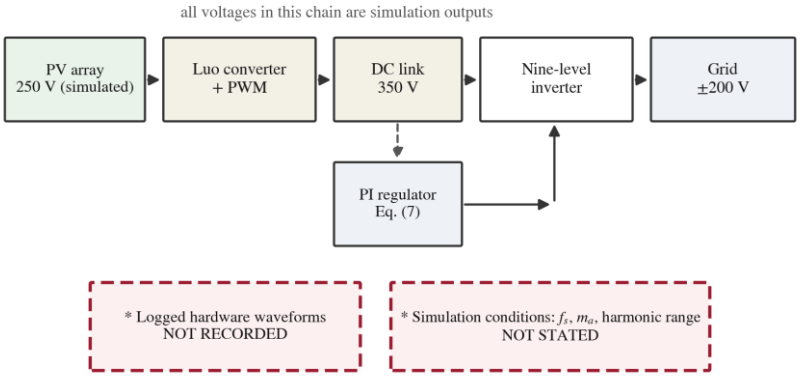

Figure 2: The conversion chain. Every voltage shown is a simulation output; the two items at the foot of the figure are what the record does not contain.

The record does not state the switching frequency, the modulation index, the passive element values, the switching-angle scheme, whether an output filter was present, or the harmonic order to which distortion was evaluated. These omissions are carried forward into Section V-D, where their consequence is quantified.

2. Study Elements as Documented

Table 3. Study Elements and the Evidence for Each

Element	Form	Evidence available
PV array model	Simulink	waveform
Luo converter	Simulink and hardware	waveform; photograph
Nine-level inverter	Simulink and hardware	waveform; photograph
PI DC-link regulator	Simulink	waveform
PWM generator	Simulink and hardware	waveform; photograph
Grid interface	Simulink	waveform
Oscilloscope capture	Hardware	photograph of the display only

A photograph of an oscilloscope display is evidence that the instrument was connected and that a waveform appeared. It is not a measurement, because no numeric value can be extracted from it with known accuracy and no spectrum can be computed from it.

3. Hardware

A hardware prototype was constructed and photographed, with an oscilloscope displaying converter and inverter outputs. The record contains photographs of those displays; it does not contain logged waveform data, a measured spectrum or any numeric hardware result. The hardware therefore demonstrates construction and operation, not performance.

Results and Verification

1. Reported Values

Table 4 lists the quantitative results exactly as reported. All are simulation outputs.

Table 4. Reported Simulation Results

Quantity	Value	Status
Converter input voltage	250 V	simulated
Converter output voltage	350 V	simulated
Grid voltage range	minus 200 to plus 200 V	simulated
Total harmonic distortion	4.9 %	simulated
Inverter levels	9	design value

2. Verifying the Conversion Ratio

The reported voltages give

$$\frac{V_o}{V_{in}} = \frac{350}{250} = 1.40 \tag{8}$$

and inverting the two candidate transfer functions gives the duty ratio each would require:

$$D_{boost} = 1 - \frac{V_{in}}{V_o} = 0.286, \quad D_{buck\text{-}boost} = \frac{V_o}{V_{in} + V_o} = 0.583 \tag{9}$$

Both are comfortably within the practical range, so the reported voltage pair is self-consistent with either topology and reveals no error. It also, however, does not identify which transfer function the model implemented, a point worth recording because the Luo converter is described in the text as a buck-output topology while the application is voltage enhancement. Stating the duty ratio alongside the voltages in any future report would remove the ambiguity immediately.

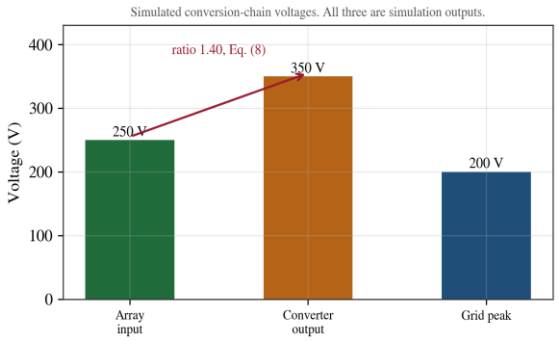

Figure 3: Simulated conversion-chain voltages. The ratio 1.40 is consistent with either candidate transfer function.

3. The Distortion Power Factor

Applying Eq. (6) to the reported distortion gives a distortion power factor of 0.9988. This is computed here rather than reported, and it inherits every condition attached to the distortion figure itself: if the underlying value changes with the harmonic range, so does this one.

4. How Much the Harmonic Range Matters

The record notes that 4.9 % clears a five per cent figure by 0.1 percentage points, and observes that a margin this thin is sensitive to the conditions of measurement. That observation is correct, and this revision makes it quantitative by evaluating Eq. (4) directly for the waveform in question.

Taking an unfiltered nine-level staircase with half-height switching angles, which places the four angles at 7.18, 22.02, 38.68 and 61.04 degrees, and summing Eq. (10) to successively higher orders gives the values in Table 5. Fig. 4 plots the cumulative curve.

Table 5. Distortion of an Unfiltered Nine-Level Staircase Against Harmonic Range (Computed Here)

Harmonic range summed	Distortion	Remark
to h = 7	1.3 %	Only the lowest orders included
to h = 15	4.1 %	Just below the reported 4.9 %
to h = 25	7.3 %	Just above the reported figure and above 5 %
to h = 49	8.3 %	The range IEEE 519 prescribes
to h = 99	8.8 %	Effectively converged

Computed from Eqs. (4) and (10) for an unfiltered equal-step nine-level staircase with half-height switching angles and no output filter. This is one specific angle-selection scheme; optimised angles or an output filter, both of which a grid-connected design would normally include, would give lower values. The table shows the sensitivity of a distortion figure to its harmonic range, not a prediction of what this model should have produced.

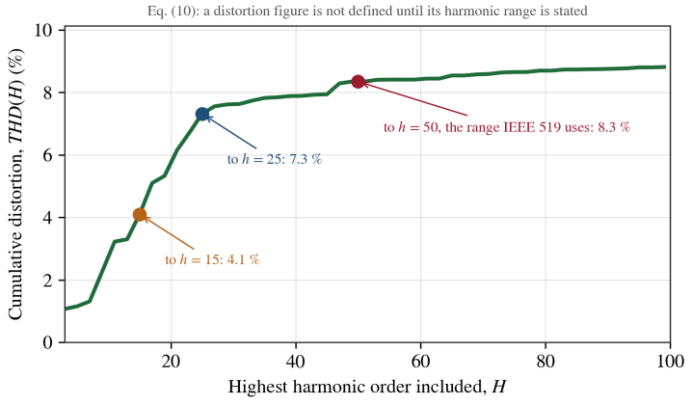

Figure. 4: Cumulative distortion against the highest harmonic order included, from Eq. (10), for an unfiltered nine-level staircase.

The consequence is sharper than the original observation. The same waveform reads 4.1 % or 8.3 % depending on nothing but where the summation stops, and the reported 4.9 % lies inside that band. Three readings are therefore all consistent with the record as it stands: the model summed over a limited harmonic range, of order the fifteenth to the twentieth; or it included an

output filter, which a grid-connected inverter would normally have and which would attenuate the higher orders; or it used optimised rather than half-height switching angles. The record states none of the three, so the figure cannot be interpreted, and this paper does not assert that it is either correct or incorrect.

What can be said is that the margin claimed for it is not robust. If the evaluation stopped short of the fiftieth harmonic and no filter was modelled, the same design assessed as the standard prescribes would not clear five per cent. Fig. 5 places the reported point against the trend for unfiltered staircases across level counts, which shows the same thing from another direction: 4.9 % sits below the unfiltered nine-level value and closer to what an unfiltered fifteen-level synthesis would give.

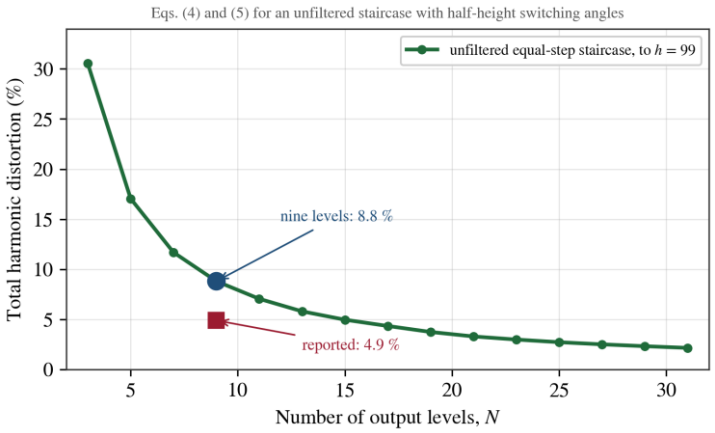

Figure 5: Distortion against inverter level count for unfiltered staircases, from Eqs. (4) and (5). Only the square marker is a reported result; the curve is computed here.

5. Which Limit Applies Is Also Undetermined

A second ambiguity compounds the first. Table II shows that the five per cent the record recalls is the voltage distortion limit for systems above 1 kV and, separately, the current total demand distortion limit; for a low-voltage connection at or below 1 kV the voltage distortion limit is 8 %. Whether the reported 4.9 % is a voltage or a current distortion is not stated, and if it is a current figure then it is a total harmonic distortion referred to the fundamental, whereas the standard limits total demand distortion referred to the demand current, which is a different denominator.

The stated margin of 0.1 percentage points is therefore not a well-defined margin. Against the 8 % voltage limit applicable to a low-voltage connection the margin would be 3.1 percentage points, which is comfortable; against a current total demand distortion limit the comparison cannot be made at all without the demand current. Establishing compliance requires naming the quantity, the voltage class and the demand current, none of which the record does, and this paper accordingly asserts no compliance.

6. Internal Inconsistencies in the Record

Two statements in the project record do not match the design and are reported rather than reconciled. The future scope proposes extension to a thirty-one-level inverter without presenting the device-count and gate-drive complexity that such an extension entails; a thirty-one-level synthesis requires fifteen independent switching angles and a correspondingly larger switch and DC-source count, and the trade-off should be argued rather than asserted. The conclusion cites a fuel cell, which appears nowhere in the design, the model or the hardware. Neither statement affects the results above, but both would mislead a reader about the scope of the work, and both are excluded from the conclusions of this paper.

7. What the Study Supports

Table 6 states the position quantity by quantity, with the provenance of each figure.

Table 6. Simulated, Computed and Absent Quantities

Quantity or capability	Value	Status
Converter voltage ratio	1.40	computed here from simulated values
Implied duty ratio, boost form	0.286	computed here
Implied duty ratio, buck-boost form	0.583	computed here

Simulated distortion	4.9 %	simulated
Distortion power factor	0.9988	computed here from the simulated value
Unfiltered nine-level distortion to h = 49	8.3 %	computed here, Eq. (10)
Hardware constructed	yes	photographed
Measured hardware voltage	—	not recorded
Measured hardware distortion	—	not recorded
Measured converter efficiency	—	not measured
Switching frequency and modulation index	—	not stated
Switching-angle scheme	—	not stated
Presence of an output filter	—	not stated
Harmonic range of the distortion figure	—	not stated
Which transfer function was modelled	—	not stated
Voltage class and demand current	—	not stated; compliance undetermined
Thirty-one-level proposal and fuel cell	—	inconsistent with the design; excluded

Discussion

This study is the strongest of its group in one respect and the weakest in another. It produced real quantitative results and they survive arithmetic checking: the voltage ratio is consistent, both implied duty ratios are practical, and the distortion power factor follows correctly. What it lacks is any connection between those numbers and the hardware standing next to them.

1. The Validation Gap Is Unusually Cheap to Close

In most of the systems examined in this group, closing the measurement gap requires new instrumentation. Here it does not. An oscilloscope was already connected to the prototype and a waveform was already displayed; the only difference between a photograph and a validated model is that the instrument's record was not saved. Modern digital oscilloscopes export waveform data to a memory device, and a distortion figure computed from that export could be compared directly against the simulated 4.9 % under a stated harmonic range. The validation gap in this work is a matter of pressing a different button.

2. Qualitative Position

Table 7 sets out the structural properties that can be asserted, each with the relation or source that supports it.

Table 7. Qualitative Properties and Their Basis

Feature	Property	Basis
Multilevel synthesis	Distortion falls as level count rises	[1], Eqs. (4), (5), Fig. 5
Voltage-lift stage	High gain without extreme duty ratios	[3]
Reported voltage pair	Self-consistent with either transfer function	Eqs. (8), (9)
Distortion figure	Not defined until its harmonic range is stated	Eq. (10), Table V
Applicable limit	Depends on quantity and voltage class	[6], Table II
PI DC-link loop	Sets modulation index from link error	Eq. (7)
Hardware evidence	Photographs demonstrate operation, not performance	Table III

Limitations

The following limitations bound every claim made in this paper.

- Every reported performance value is a simulation output. No hardware measurement of voltage, current, distortion, efficiency or power factor was recorded, so the model is unvalidated.
- The hardware evidence consists of photographs of an oscilloscope display, from which no numeric value can be extracted with known accuracy and no spectrum can be computed.

- The switching frequency, modulation index, passive element values, switching-angle scheme, presence of an output filter and harmonic range are all unstated, so the simulation cannot be reproduced and its distortion figure cannot be interpreted.
- The computed values in Table V are for one specific angle-selection scheme with no output filter. They demonstrate the sensitivity of distortion to harmonic range; they are not a prediction of what this model should have produced, and they do not establish that the reported 4.9 % is wrong.
- The limits in Table II are published criteria, not measurements. Which of them applies to this design cannot be determined, because the record states neither the quantity measured nor the voltage class nor the demand current.
- This paper takes no position on the correctness of the simulation itself, which cannot be checked without the model's parameters.
- The thirty-one-level proposal and the fuel-cell reference are inconsistent with the design and are excluded from every claim.

Proposed Validation Path

Fig. 6 shows what would connect the model to the hardware. The path is short because the instrument is already in place.

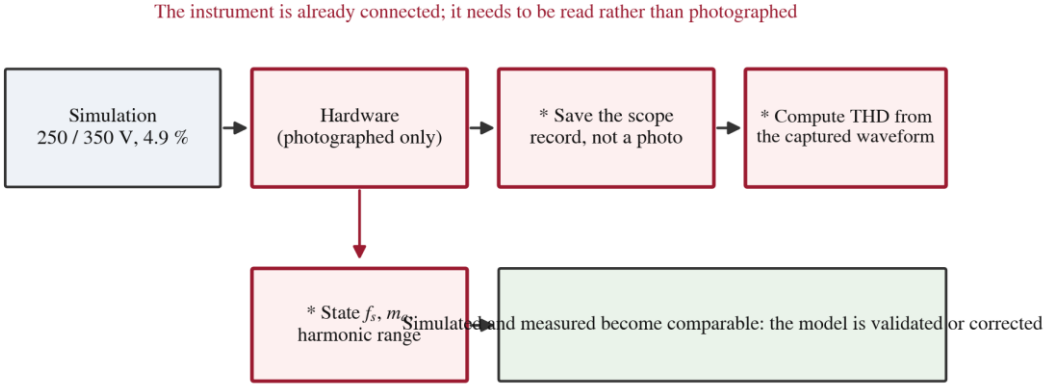

Figure 6: Validation path. The instrument is already connected; it needs to be read rather than photographed.

1. Measurement Plan

Table 8 sets out the steps, and Table 9 records every figure in the study with its provenance so that none is carried forward as a measurement.

Table 8. Measurement Plan Required to Validate the Model

Step	Method	What it yields
Record the hardware waveforms	Export oscilloscope data rather than photographing the display	A waveform from which distortion can be computed
Compute distortion from the export	Fourier analysis to a stated harmonic order	A measured figure comparable with the simulated one
State the simulation conditions	Switching frequency, modulation index, passive values, angle scheme, filter, harmonic range	Reproducibility, and an interpretable distortion figure
State the quantity and voltage class	Whether voltage or current distortion, at what voltage, with the demand current	The applicable limit from Table II
Measure converter efficiency	Log input and output power together	An efficiency alongside the conversion ratio
Resolve the topology description	State which transfer function the Luo stage implements and give the duty ratio	Removes the ambiguity of Section V-B

Justify or drop the thirty-one-level proposal	Present the device-count and complexity trade-off	A supported extension rather than an assertion
Correct the record	Remove the fuel-cell statement or add the subsystem	Internal consistency

Table 9. Figures and Their Provenance

Item	Value	Status
Input and output voltage	250 / 350 V	simulated
Grid voltage peak	plus and minus 200 V	simulated
Total harmonic distortion	4.9 %	simulated; harmonic range unstated
Voltage ratio and duty ratios	1.40; 0.286 / 0.583	computed here
Distortion power factor	0.9988	computed here
Unfiltered staircase distortion	4.1 % to 8.8 % by range	computed here, Eq. (10)
Voltage distortion limit at or below 1 kV	8.0 %	standard [6]
Current total demand distortion limit	5.0 %	standard [6]

All performance values are simulation outputs. No hardware measurement was recorded in this campaign, and no compliance with any harmonic standard is asserted.

Conclusion

A grid-connected photovoltaic conversion chain combining a Luo converter with a nine-level inverter and a proportional-integral regulated DC link was designed, modelled in simulation and realised in hardware. The study produced quantitative results, and these were verified rather than restated: the simulated boost from 250 V to 350 V is a ratio of 1.40, requiring a duty ratio of 0.286 under a boost transfer function or 0.583 under the buck-boost form, both practical, so the reported pair is self-consistent though it does not identify which transfer function was modelled. The simulated total harmonic distortion of 4.9 % corresponds to a distortion power factor of 0.9988, computed here.

This revision replaced the comparison against a remembered five per cent with the standard as written, and found two distinct ambiguities. First, evaluating the Fourier series of an unfiltered nine-level staircase shows that the same waveform yields 4.1 % when summed to the fifteenth harmonic and 8.3 % when summed to the fiftieth, which is the range the standard prescribes; the reported 4.9 % lies inside that band, so it is consistent with a limited harmonic range, with an output filter, or with optimised switching angles, and the record distinguishes none of the three. Second, the applicable limit depends on which quantity and which voltage class is meant: for a low-voltage connection the voltage distortion limit is 8 %, not 5 %, while the 5 % figure governs current total demand distortion referred to a different denominator. The claimed margin of 0.1 percentage points is therefore not a well-defined margin, and no compliance is asserted here.

The principal limitation is that the numbers and the hardware are disjoint: every reported value is a simulation output, while the hardware produced photographs of an oscilloscope rather than recorded data, so the model remains unvalidated. Two inconsistencies in the record, being a thirty-one-level inverter in the future scope and a fuel cell in the conclusion, neither present in the design, were reported rather than reconciled silently. Closing the validation gap requires only that the instrument already in use be read rather than photographed, which makes this among the cheapest validation gaps in the group to close.

Future Work

Several extensions follow directly from the limitations above.

- Record the hardware waveforms-Export oscilloscope data rather than photographs, and compute distortion from the captured waveform so that the model can be validated or corrected.
- State the simulation conditions-Report the switching frequency, modulation index, passive values, switching-angle scheme, whether an output filter was included, and the harmonic range over which distortion was evaluated. Without the last three the reported figure cannot be interpreted at all.
- Name the quantity and the voltage class-State whether the distortion is a voltage or a current figure, at what voltage, and

with what demand current, so that the applicable limit in Table II can be identified.

- Measure converter efficiency-Log input and output power together, so that the conversion stage carries a measured efficiency alongside its ratio.
- Resolve the topology description-State which transfer function the Luo stage implements and give the duty ratio, removing the ambiguity identified in Section V-B.
- Justify or drop the thirty-one-level proposal-If higher level counts are intended, present the device-count and complexity trade-off that motivates them.
- Correct the record-Remove the fuel-cell statement from the conclusion or add the subsystem to the design.

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