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An Artificial-Neural-Network-Controlled Single-Phase Unified Power Flow Controller for Power-Quality Mitigation

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Abstract

This paper presents the design and hardware realisation of a single-phase unified power flow controller whose DC-link regulation is performed by an artificial neural network, with reference extraction by decoupled double synchronous reference frame theory and gating by a hysteresis current controller. The converter chain, the series and shunt compensator control laws, the reference-frame transformation and the network structure are formalised in full, and a working laboratory prototype was constructed around a dsPIC30F4011 digital signal controller with TLP250-driven MOSFET bridges and a regulated auxiliary supply. The paper is explicit about what the campaign establishes and what it does not. The prototype was completed and connected to a digital storage oscilloscope, but no waveforms, harmonic spectrum, THD, power factor, efficiency, or simulation data were recorded. Therefore, the claimed reduction in source-current distortion cannot be evaluated or quantified from this work. Statements in the project record describing good transient response with less overshoot are identified as expectations drawn from the literature rather than observations of this prototype. This revision adds two quantitative elements. The distortion limits the compensator would have to meet are stated from IEEE Std 519-2022 rather than described as application-dependent, and the distinction between total harmonic distortion, which the paper's own defining relation expresses, and total demand distortion, which the standard actually limits, is made explicit; the two differ whenever the load is below its rated demand, so a compliant-looking figure computed one way can conceal non-compliance the other. The hysteresis design compromise is also evaluated numerically, showing that for plausible link voltages and coupling inductances the band that the record does not document sets the switching frequency across more than an order of magnitude. The paper contributes a complete and traceable design description, a precise account of the four measurements needed to close the gap, and an assessment framework in which the network, the extraction stage and the hysteresis controller can each be evaluated separately.

Nomenclature

Symbol	Meaning
v_s, i_s	Source voltage (V) and source current (A)
v_L, i_L	Load voltage (V) and load current (A)

V_{dc}	DC-link capacitor voltage (V)
V_{se}, I_{sh}	Series injected voltage (V) and shunt current (A)
i_d, i_q	Direct- and quadrature-axis current (A)
i_α, i_β	Stationary-frame orthogonal current pair (A)
ω, θ, δ	Fundamental angular frequency (rad/s), phase angle and injection angle
THD, TDD	Total harmonic distortion and total demand distortion (%)
I_h, I_1, I_L	Harmonic, fundamental and maximum demand load current (A)
h	Harmonic order
PF	Displacement power factor
k_p, k_i	Proportional and integral gains
w_{ij}, b_j	Network weights and biases
Δi, f_{sw}	Hysteresis band width (A) and switching frequency (Hz)
L, C	Coupling inductance (H) and DC-link capacitance (F)

Introduction

Power quality at the point of common coupling is degraded principally by nonlinear loads, which draw non-sinusoidal current and so distort the supply voltage across the source impedance [7], [4]. Passive filters address this only at the frequencies for which they are tuned, and their performance drifts with load and with supply impedance; active compensation, in which a converter injects a current or voltage that cancels the disturbance, adapts to changing conditions and is now the standard approach for demanding loads [6], [3].

The unified power flow controller combines both forms of compensation. A shunt converter exchanges reactive current with the point of common coupling and holds the DC-link voltage; a series converter injects a controlled voltage in line with the feeder, so that real and reactive power flow can be adjusted independently [1], [2]. The control problem is therefore twofold: extracting an accurate reference from a distorted waveform, and regulating the DC link through load transients.

This paper reports a single-phase unified power flow controller addressing both: decoupled double synchronous reference frame theory extracts the reference, and an artificial neural network regulates the DC-link voltage. A hardware prototype was built around a dsPIC30F4011 controller. The paper documents the design completely and is deliberately explicit that the performance claims such a design invites were not measured in this campaign.

1. Problem Statement

Custom-power literature reports distortion reductions and settling times obtained from well-instrumented benches or from simulation. Undergraduate prototype reports of the same architectures very often present a photograph of working hardware and then restate the literature's performance figures as though they were outcomes of the build. The gap addressed here is the separation between a design that is genuinely complete and a performance claim that requires instrumentation the campaign did not deploy.

2. Objectives

The specific objectives of the work are as follows:

- To formalise the single-phase unified power flow controller control chain in full: reference extraction, series and shunt laws, DC-link dynamics and network regulation.
- To realise the design in hardware and to document the controller, gate-drive, switching and auxiliary-supply stages as built.
- To state explicitly which performance quantities were not recorded, and why the distortion-reduction claim is therefore not evaluable from this work.
- To state the distortion limits such a compensator would have to meet, in the units the governing standard actually uses.
- To evaluate the hysteresis design compromise numerically, so that the undocumented band is seen to matter rather than assumed not to.
- To specify a measurement plan and a staged assessment that would attribute any improvement to the network, the extraction stage or the hysteresis controller separately.

3. Scope and Delimitation

The study covers the control formalisation, the hardware realisation and the specification of the measurements that were absent. It excludes any claim of total harmonic distortion, total demand distortion, settling time, overshoot, power factor, converter efficiency or switching frequency for this build, because none was measured or documented. It excludes any comparison between the network regulator and a

proportional-integral regulator, because no transient was recorded for either. And it excludes the transient-response statement found in the project record, for the reason given in Section V-C.

4. Contributions

1. A complete formalisation of the single-phase unified power flow controller control chain: reference extraction, series and shunt laws, DC-link dynamics and network regulation.
2. A documented hardware realisation with the controller, gate-drive, switching and auxiliary-supply stages specified as built.
3. An explicit statement that no waveform, spectrum, distortion, power-factor or efficiency data were recorded, and that the distortion-reduction claim is therefore not evaluable from this work.
4. A statement of the applicable distortion limits from IEEE Std 519-2022, new to this revision, together with the distinction between total harmonic distortion and total demand distortion that determines whether a reported figure means anything.
5. A numerical evaluation of the hysteresis design compromise, new to this revision, showing the range over which the undocumented band sets the switching frequency.
6. A four-measurement plan sufficient to make the assessment quantitative, with the block-level tests that would attribute any improvement to the network, the extraction stage or the hysteresis controller separately.

The remainder of the paper is organised as follows. Section II reviews related work and fixes the applicable limits. Section III develops the control relations. Section IV describes the prototype. Section V reports the results and their honest reading. Section VI discusses the findings, Section VII states the limitations, and Section VIII gives the assessment framework. Sections IX and X give the conclusion and the future scope.

Related Work

Gyugyi [1] introduced the unified power flow controller concept and established the independence of real- and reactive-power control obtainable from combined series and shunt injection; Hingorani and Gyugyi [2] give the standard treatment of the flexible AC transmission system controllers within which the device sits. For distribution-level custom power devices, Ghosh and Ledwich [3] develop the compensator structures and control laws directly comparable to the present single-phase realisation.

On reference extraction, Akagi and colleagues [4] formalised instantaneous power theory, and Rodríguez and colleagues [5] developed the decoupled double synchronous reference frame used here, showing that it separates positive- and negative-sequence components under unbalanced and distorted supply, which is the property that motivates its use in Section III. Singh and colleagues [6] survey active-filter control including hysteresis current regulation, and note the trade-off between band width, switching frequency and residual ripple that Eq. (7) makes explicit and that Section V-D evaluates. Dugan and colleagues [7] give the standard treatment of power-quality phenomena at the point of common coupling.

Table I: Representative Related Work and its Relation to This Study

Ref.	Year	Focus and scope	Method and validation	Relation to this work
[1]	1992	UPFC concept and capability	Analysis; converter theory	Defines the device realised here
[2]	2000	FACTS controllers	Reference text	System context for series and shunt action
[3]	2002	Custom power devices	Control design; simulation	Distribution-level compensator basis
[4]	1984	Instantaneous reactive power theory	Analysis; experiment	Foundation of reference extraction
[5]	2007	Decoupled double synchronous reference frame	Analysis; experiment	The extraction stage adopted here
[6]	1999	Active filter control review	Survey	Hysteresis control trade-offs
[7]	—	Power-quality phenomena	Reference text	Distortion mechanism at the PCC

[8]	2022	IEEE Std 519 harmonic control	Recommended practice	The limits a result must be compared against

Two corrections have been made to this table in the present revision. Reference [7] was cited in the introduction of an earlier draft but omitted from the table, and has been restored. An entry appearing in an earlier draft as a citation for neural DC-link regulation pointed to no identifiable publication, being a note referring the reader back to the active-filter survey; it has been removed rather than retained as an unverifiable citation, and the motivation for the network regulator is now attributed in the text to the general adaptive-control argument rather than to a specific source that could not be located.

1. The Limits a Result Would Have to Meet

The central claim such a design invites is a reduction in source-current distortion. That claim is only meaningful against a stated limit, and the governing document is IEEE Std 519, of which the 2022 edition is current and supersedes the 2014 revision. Table 2 states the applicable values.

Table 2. Distortion Limits from IEEE Std 519-2022

Quantity	Limit	Applicability
Voltage, individual harmonic	5.0 %	Systems at or below 1.0 kV, at the point of common coupling
Voltage, total harmonic distortion	8.0 %	Systems at or below 1.0 kV
Voltage, individual harmonic	3.0 %	Systems above 1.0 kV and up to 69 kV
Voltage, total harmonic distortion	5.0 %	Systems above 1.0 kV and up to 69 kV
Current, 3 ≤ h < 11	4.0 % of I_L	Short-circuit to demand-current ratio below 20
Current, 11 ≤ h < 17	2.0 % of I_L	Short-circuit to demand-current ratio below 20
Current, 17 ≤ h < 23	1.5 % of I_L	Short-circuit to demand-current ratio below 20
Current, 23 ≤ h < 35	0.6 % of I_L	Short-circuit to demand-current ratio below 20
Current, 35 ≤ h ≤ 50	0.3 % of I_L	Short-circuit to demand-current ratio below 20
Current, total demand distortion	5.0 %	Short-circuit to demand-current ratio below 20

Values are the limits published in IEEE Std 519-2022 [8]. Even harmonics of order six and below are limited to half the tabulated values, and current distortion producing a direct-current offset is not permitted. The limits apply at the point of common coupling between utility and user, and current limits are the user's responsibility while voltage limits are the utility's. Nothing in this table was measured on the prototype described in Section IV.

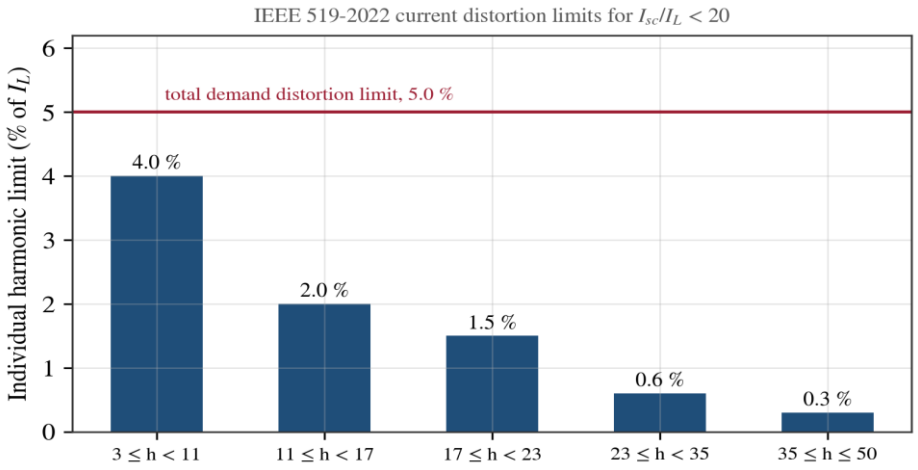

Figure 1: Current distortion limits from IEEE Std 519-2022 for a short-circuit to demand-current ratio below 20, with the total demand distortion limit marked.

System Modelling and Control

1. Compensation Objective and the Units It Is Judged In

For a source current containing harmonics of order h, total harmonic distortion is defined as

$$THD = \frac{\sqrt{\sum_{h\geq 2} I_h^2}}{I_1} \times 100\,\% \qquad (1)$$

and the objective of the compensator is to reduce Eq. (1) at the source while holding the load supplied. Evaluating it requires the harmonic amplitudes, that is, a spectrum of the measured source current; this is the measurement identified as missing in Section V-B.

A distinction that matters for any comparison with the limits of Table II must be drawn here, because the two quantities are routinely conflated. Equation (1) refers the harmonic content to the fundamental current actually flowing. The standard instead limits total demand distortion, which refers the same harmonic content to the maximum demand load current,

$$TDD = \frac{\sqrt{\sum_{h\geq 2} I_h^2}}{I_L} \times 100\,\% \qquad (10)$$

The two coincide only when the load is drawing its rated demand. At light load the fundamental is small, so Eq. (1) can be large while Eq. (10) is comfortably within limits; conversely a figure computed by Eq. (1) at heavy load understates nothing but is not the quantity the standard bounds. A reported distortion figure is therefore not interpretable unless the load condition and the reference current are stated alongside it, which is the reporting convention recommended in Section VIII-C.

2. Reference Extraction

A single-phase quantity is first extended to an orthogonal pair by a quarter-cycle delay, giving a stationary-frame pair, and then rotated into synchronous coordinates,

$$i_d = i_\alpha \cos\theta + i_\beta \sin\theta,\quad i_q = -i_\alpha \sin\theta + i_\beta \cos\theta,\quad \theta = \omega t \qquad (2)$$

In the decoupled double synchronous reference frame formulation, two frames rotating at plus and minus the fundamental angular frequency are used simultaneously and cross-coupled through a decoupling network, so that the oscillating component appearing in one frame due to the opposite sequence is cancelled rather than filtered [5]. The direct components of the positive-frame outputs are the fundamental components, and the reference compensating current follows as

$$i^* = i_L - \bar{i}_{d,1} \cos\theta \qquad (3)$$

where the barred term is the extracted fundamental active component. The practical merit of Eqs. (2) and (3) is that the reference retains the harmonic content in antiphase, so injecting it cancels the load harmonics at the point of common coupling.

3. Series and Shunt Control Laws

The series converter injects a voltage in the feeder,

$$v_s = v_L + V_{se} \angle \delta \qquad (4)$$

whose in-phase component adjusts real power flow and whose quadrature component adjusts reactive flow; the locus available for the injected voltage is the circle of Fig. 2, bounded by the converter rating,

$$|V_{se}| \leq V_{se,\max}, \qquad P = \frac{V_s V_L}{X} \sin\delta \qquad (5)$$

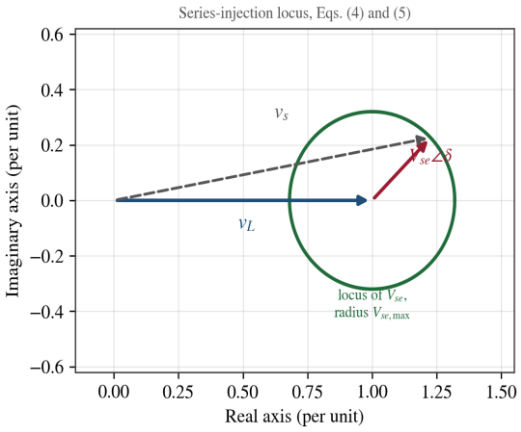

Figure 2: Series-injection locus available to the controller from Eqs. (4) and (5); the converter rating bounds the circle.

The shunt converter simultaneously supplies the real power drawn by the series branch and maintains the DC link, so that at steady state

$$P_{sh} = P_{se} + P_{loss}, \qquad C V_{dc} \frac{dV_{dc}}{dt} = P_{sh} - P_{se} - P_{loss} \qquad (6)$$

Equation (6) is the plant that the network regulates.

4. Hysteresis Current Control

Gating is produced by comparing the measured injected current with its reference within a band,

$$S = 1 \ (i_c < i^* - \Delta i/2); \qquad S = 0 \ (i_c > i^* + \Delta i/2) \qquad (7)$$

The band sets the current ripple directly and the switching frequency inversely, so it is the principal design compromise between tracking accuracy and switching loss. To a first order, for a converter of link voltage V_{dc} feeding a coupling inductance L, the maximum switching frequency is

$$f_{sw,\max} \approx \frac{V_{dc}}{4 L \Delta i} \qquad (11)$$

Equation (11) is evaluated in Section V-D, where it is used to show that the band the record does not document is not a minor omission.

5. Network DC-Link Regulator

The regulator is a feed-forward network with one hidden layer. For hidden node j and output node k,

$$h_j = f\left(\sum_i w_{ij} x_i + b_j\right), \quad y_k = \sum_j w_{jk} h_j + b_k \tag{8}$$

with a sigmoidal activation

$$f(u) = \frac{1}{1 + e^{-u}} \tag{9}$$

The network input vector is the DC-link voltage error and its rate of change, and the output is the active current command. The network is trained offline and the weights are then fixed in the controller. It should be stated plainly that a network of this form with these inputs is functionally an adaptive proportional-derivative surface on the same two signals a conventional regulator uses, and that demonstrating an advantage over a tuned proportional-integral controller requires a measured transient comparison, which this campaign did not perform.

Hardware Realisation

1. Architecture

Fig. 3 shows the prototype. The single-phase supply feeds the load through the series transformer; the shunt branch is connected at the point of common coupling. Both converters are MOSFET bridges gated from a dsPIC30F4011 digital signal controller through TLP250 optically-isolated drivers, and a common DC-link capacitor couples them. Sensing of source voltage and current is returned to the controller's analogue inputs, and a transformer, bridge and regulator chain supplies the plus and minus 15 V and 5 V rails. The two items shown as absent at the foot of the figure are the ones on which the whole of Section V turns.

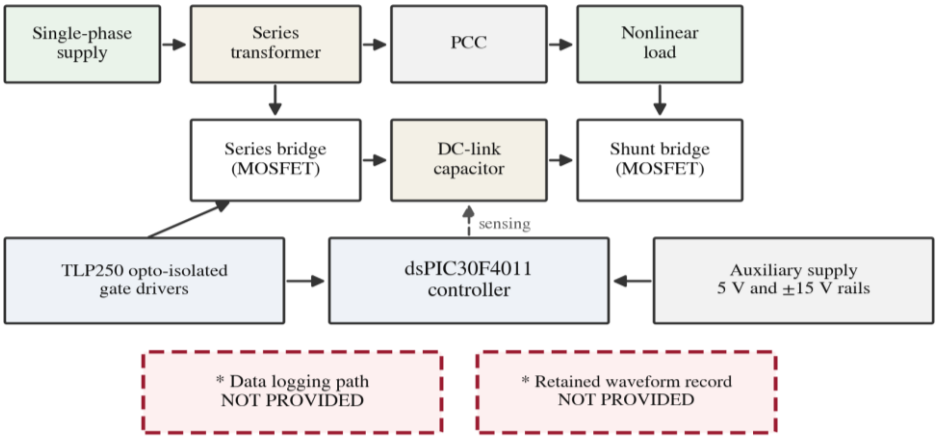

Figure 3: Prototype architecture. Sensing returns to the controller; no logging path was provided at any node.

2. Apparatus

Table 3 lists the prototype as documented.

Table 3. Prototype as Documented

Item	Type / rating	Quantity
Digital signal controller	dsPIC30F4011	1
Gate driver	TLP250, opto-isolated	4 or more
Switching device	MOSFET, IRF840 class	4 or more
Series transformer	Rating not stated in the record	1
DC-link capacitor	Value not stated in the record	1
Coupling inductance	Value not stated in the record	—
Auxiliary supply	Bridge and regulator, 5 V and ±15 V	1
Oscilloscope	Digital storage	1

The DC-link voltage, the DC-link capacitance, the coupling inductance, the hysteresis band and the resulting switching frequency are all absent from the record. The first three are needed to evaluate Eq. (6); the last two are the subject of Section V-D.

3. Procedure

- Construct the auxiliary supply and verify the 5 V and 15 V rails.
- Program the controller with the reference extraction, network regulator and hysteresis gating; verify gate pulses at the driver outputs.
- Connect the series and shunt bridges to the DC link and the series transformer,

and energise with a nonlinear load at the point of common coupling.
- Observe source voltage and current on the oscilloscope.

Results

1. What the Campaign Established

The prototype was built and energised, the controller was programmed, and the converters were driven through their isolated gate drivers with an oscilloscope connected at the source. That is the extent of the observed result, and it is reported without extension. Fig. 4 shows the position by category.

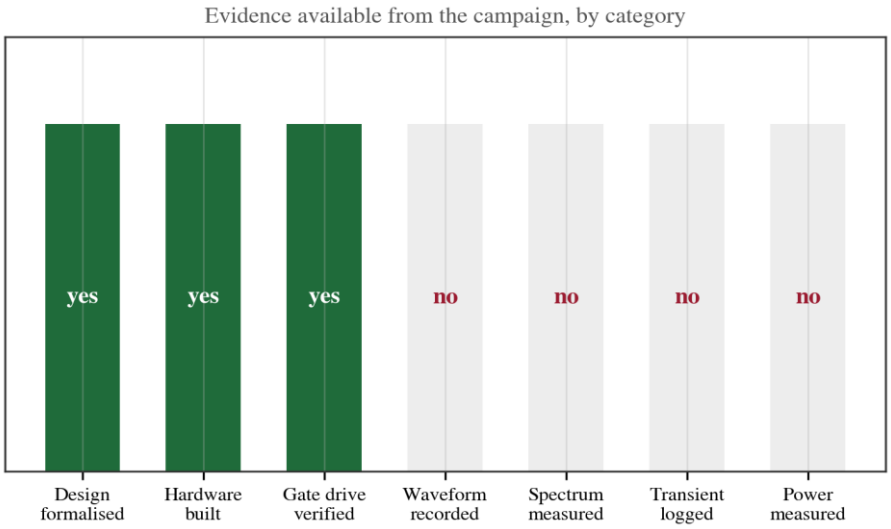

Figure 4: Evidence available from the campaign, by category.

2. Why No Distortion, Power Factor or Efficiency Is Reported

Evaluating the compensator requires four quantities, none of which was recorded:

- The source-current harmonic spectrum with the compensator disabled, without which the baseline of Eq. (1) is unknown;
- The same spectrum with the compensator enabled, without which the improvement is unknown;
- The DC-link voltage through a load step, without which the network's regulation performance and any comparison with proportional-integral control is unavailable;
- Simultaneous input and output power, without which efficiency cannot be computed.

Although a digital storage oscilloscope was connected, no waveform record, screen capture or spectrum was retained, and no simulation figures were kept in the project record. Consequently no distortion value, settling time, power factor or efficiency appears anywhere in this paper, and none is estimated. Fig. 5 shows only the form such a result would take.

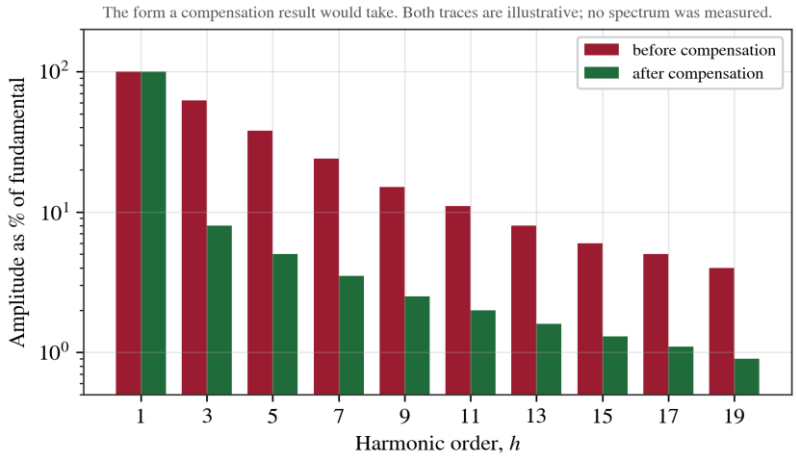

Figure 5: The form a compensation result would take: source-current spectrum before and after. Both traces are illustrative; no spectrum was measured.

3. On the Transient-Response Statement

The project record states that simulation results show good transient response with less overshoot and reduced oscillation. No simulation model, parameter set or output figure accompanies that statement in the record, and none was available for this paper. It is therefore reported here as an expectation consistent with the cited literature [3], not as an observation of this design, and it is excluded from the conclusions.

4. The Undocumented Hysteresis Band Is Not a Minor Omission

Table 3 records that the hysteresis band and the resulting switching frequency are undocumented. Equation (11) shows what that omission costs. Table 4 evaluates it for plausible link voltages and coupling inductances, and Fig. 6 plots the relation.

Table 4. Maximum Switching Frequency from Eq. (11) (Computed from Assumed Values)

Link voltage and inductance	Δi = 0.1 A	Δi = 0.25 A	Δi = 0.5 A	Δi = 1.0 A
100 V, 5 mH	50 kHz	20 kHz	10 kHz	5 kHz
100 V, 10 mH	25 kHz	10 kHz	5 kHz	2.5 kHz
200 V, 10 mH	50 kHz	20 kHz	10 kHz	5 kHz

Computed from Eq. (11) for assumed link voltages and coupling inductances. None of these values is documented for this build, and Eq. (11) is a first-order estimate that neglects back-electromotive force variation over the fundamental cycle, so the figures bound an order of magnitude rather than predict a value.

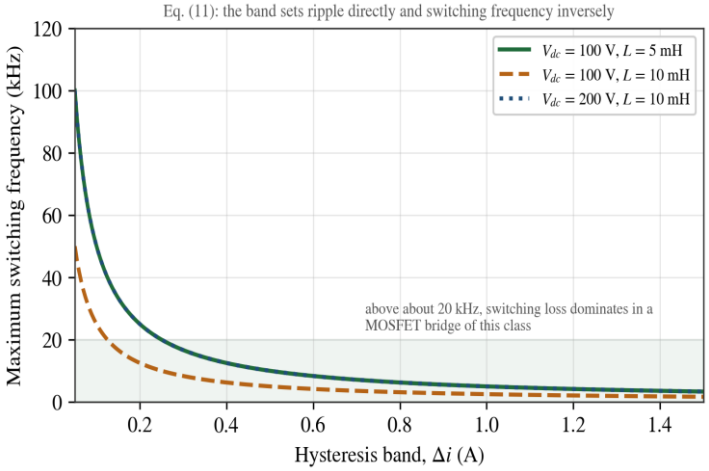

Figure 6: Maximum switching frequency against hysteresis band from Eq. (11), for three combinations of link voltage and coupling inductance.

The reading is that the band spans the design across more than an order of magnitude of switching frequency, from a few kilohertz to tens of kilohertz, for entirely reasonable choices. At the low end the current ripple is coarse and the residual distortion the compensator leaves behind may itself be significant; at the high end the switching loss in an IRF840-class device becomes the dominant loss term and the efficiency figure, also unmeasured, would suffer. A distortion result reported without the band and the resulting frequency is therefore not reproducible, which is why both appear in the reporting conventions of Section VIII-C.

5. What the Campaign Supports

Table 5 states the position quantity by quantity.

Table 5. Built, Unmeasured and Indeterminate Quantities

Quantity or capability	Value	Status
Prototype constructed	yes	demonstrated
Controller programmed	yes	demonstrated
Gate drive verified	yes	demonstrated
Source-current spectrum	—	not recorded
Total harmonic distortion, before and after	—	indeterminate

Total demand distortion	—	indeterminate; I_L not recorded either
DC-link transient	—	not recorded
Network versus PI comparison	—	indeterminate
Power factor at the PCC	—	not measured
Converter efficiency	—	not measured
Switching frequency	—	not documented
Hysteresis band Δi	—	not documented
DC-link voltage and capacitance	—	not documented
Coupling inductance	—	not documented
Load type, rating and short-circuit ratio	—	not documented
Simulation waveforms	—	not retained
Transient-response statement	—	literature expectation, not observation
Switching-frequency range implied by Eq. (11)	2.5 to 50 kHz	computed from assumed values
Applicable current distortion limit	5.0 % total demand distortion	standard [8], not a measurement

Discussion

The design side of this work is complete in a way that many prototype reports are not: the extraction, the injection laws, the DC-link balance and the network structure are all stated, and the hardware realisation is specified down to the driver and device class. The measurement side is empty. That asymmetry is the honest summary, and the value of the paper lies in not disguising it.

1. The Network Regulator Deserves a Fair Test

It is worth being precise about what would have to be shown. A feed-forward network taking error and error-derivative as inputs spans, at fixed weights, a static nonlinear surface over the same two signals a proportional-derivative controller uses linearly. Its potential advantage is therefore that the surface may be shaped better than a straight line for the particular plant of Eq. (6), especially away from the operating point where a fixed-gain regulator is detuned. That is a real and testable proposition. It is not established by the network working, only by a paired transient in which the regulator is the sole variable, which is stage five to seven of the framework in Section VIII.

2. Qualitative Position

Table 6 sets out the structural properties that can be asserted, each with the relation or source that supports it.

Table 6. Qualitative Properties and Their Basis

Feature	Property	Basis
Series injection	Controls real and reactive flow independently	[1], Eqs. (4), (5)
Shunt branch	Supplies series real power; holds the DC link	Eq. (6)
Reference extraction	Separates sequences under distortion	[5], Eqs. (2), (3)
Hysteresis gating	Simple; variable switching frequency set by the band	Eqs. (7), (11)
Network regulator	Adaptive surface; benefit needs a paired measurement	Section VI-A
Opto-isolated drive	Protects the controller from the power stage	This work
Distortion reporting	Meaningless without load condition and reference current	Eqs. (1), (10), [8]

Limitations

The following limitations bound every claim made in this paper.

- No waveform, spectrum, distortion figure, power factor, settling time or efficiency was recorded. These quantities are indeterminate for this build, not merely uncertain, and none is estimated.
- No simulation model, parameter set or output figure was retained, so the simulated behaviour cannot be reported or compared against measurement either.

- The DC-link voltage and capacitance, the coupling inductance, the hysteresis band and the load rating are undocumented, so the design cannot be reproduced from this paper and Eqs. (6) and (11) cannot be evaluated for the actual build.
- The switching-frequency figures of Table IV use assumed values and a first-order relation that neglects back-electromotive force variation. They bound an order of magnitude rather than predict a value.
- The distortion limits of Table II are published values from IEEE Std 519-2022. They are the criteria a result would be judged against, not measurements of anything in this work, and they apply at the point of common coupling rather than at equipment terminals.
- The spectrum of Fig. 5 is illustrative of the form a result would take. Neither trace is data.
- The transient-response statement in the project record is a literature expectation and is excluded from the conclusions.
- No comparison between the network regulator and a proportional-integral regulator is offered, because no transient was recorded for either.

Proposed Assessment Framework

The design motivates the staged evaluation of Fig. 7, in which each control block is exercised separately so that any improvement can be attributed rather than assumed.

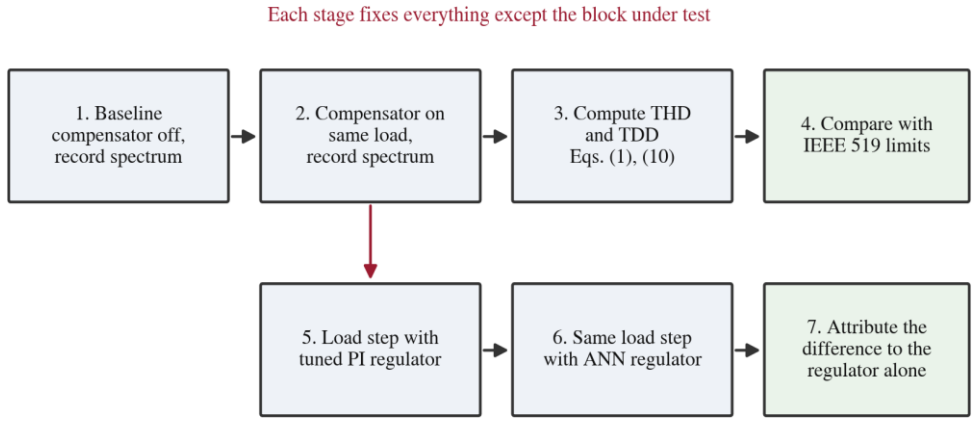

Figure 7: Staged assessment: compensation stages first, then a paired regulator comparison on the same hardware and load.

1. Attributing the Improvement

Because the extraction stage, the hysteresis gating and the network regulation act on different parts of the problem, a single end-to-end distortion figure cannot attribute credit between them. The staged sequence isolates the compensation topology first; only then is the regulator swapped between proportional-integral and network control with all else fixed, so that the difference measured is due to the regulator alone.

2. Measurement Plan

Table 7 sets out the measurements required, and Table 8 gives the context values that are standards guidance or literature rather than results.

Table 7. Measurement Plan Required to Make the Assessment Quantitative

Measurement	Method	What it yields
Baseline spectrum	Source current with the compensator disabled, under a stated load	The denominator of any improvement claim
Compensated spectrum	The same load with the compensator enabled	Distortion reduction through Eq. (1)
Record the demand current	Maximum demand load current over the measurement window	Allows Eq. (10) and comparison with Table II
DC-link transient	Repeatable load step with V_{dc} logged	Overshoot and settling time as results

Paired regulator comparison	The same step with a tuned PI regulator and with the network, all else fixed	Attributes any difference to the regulator alone
Power measurement	Simultaneous input and output voltage and current	Power factor and converter efficiency
Document the switching design	Record Δi and the observed switching-frequency range	Reproducibility; validates Eq. (11)
Retain the simulation	Preserve model, parameters and output figures	Allows measured and simulated behaviour to be compared

3. Reporting Conventions

Any future report of this system should state the load type and rating, the supply short-circuit ratio, the maximum demand current, the hysteresis band, the resulting switching-frequency range and the measurement bandwidth alongside the distortion figure, and should say whether the figure is total harmonic distortion by Eq. (1) or total demand distortion by Eq. (10). A distortion value quoted without these is not comparable with any other published result and cannot be checked against Table 2.

Table 8. Illustrative Figures (Standards and Literature, Not Results)

Item	Illustrative value	Status
Current total demand distortion limit	5.0 %	standard [8]
Voltage distortion limit at or below 1 kV	8.0 % total, 5.0 % individual	standard [8]
Active-filter distortion reduction	Wide and load-dependent	literature [6]
Switching frequency for Δi = 0.25 A	10 to 20 kHz	computed from assumptions, Eq. (11)
Measured distortion, this work	—	indeterminate
Measured efficiency, this work	—	indeterminate
Measured settling time, this work	—	indeterminate

Entries are standards guidance, literature ranges or values computed from stated assumptions, quoted for orientation only. They were not measured here and are not performance claims for this prototype.

Conclusion

A single-phase unified power flow controller with decoupled double synchronous reference frame extraction, hysteresis current control and an artificial-neural-network DC-link regulator was designed and realised in hardware around a dsPIC30F4011 controller with opto-isolated gate drives and a regulated auxiliary supply. The control chain was formalised in full, including the reference-frame transformation, the series and shunt laws, the DC-link power balance and the network structure. The prototype was built, programmed and energised with an oscilloscope connected.

Beyond that, the campaign supports no quantitative claim: no waveform record, harmonic spectrum, distortion figure, power factor, settling time or efficiency was logged, and no simulation output was retained, so the central proposition that this controller reduces source-current distortion cannot be evaluated here and no value is reported. The frequently repeated statement about good transient response was identified as a literature expectation rather than an observation of this build.

This revision added the criteria such a result would have to meet. IEEE Std 519-2022 limits current total demand distortion to 5.0 % for a short-circuit to demand-current ratio below 20, with individual harmonic limits from 4.0 % down to 0.3 % by order, and voltage distortion to 8.0 % on systems at or below 1 kV. It also limits total demand distortion rather than total harmonic distortion, and the two differ whenever the load is below rated demand, so a figure computed by the paper's own defining relation is not directly comparable with the standard unless the demand current is stated. The hysteresis design compromise was evaluated numerically and shown to set the switching frequency from a few kilohertz to tens of kilohertz across reasonable band choices, which makes the undocumented band a reproducibility failure rather than a detail.

A staged assessment framework was proposed which isolates the compensation topology before

comparing the network regulator against a tuned proportional-integral regulator on identical hardware, together with the specific measurements that would make the evaluation quantitative and the reporting conventions needed for the result to be comparable with published work.

Future Work

Several extensions follow directly from the limitations above.

- Capture the spectra-Record source-current waveforms with the compensator disabled and enabled under an identical load, and compute Eq. (1) from both.
- Record the demand current and report both measures-Log the maximum demand load current so that Eq. (10) can be evaluated and the result compared against the limits of Table II.
- Record a DC-link transient-Apply a repeatable load step and log V_{dc}, so that overshoot and settling time become results.
- Run the paired regulator comparison-Repeat that transient with a tuned proportional-integral regulator and with the network, all else unchanged.
- Measure power-Log input and output voltage and current simultaneously to obtain power factor and efficiency.
- Document the switching design-Record the hysteresis band, the link voltage, the coupling inductance and the resulting switching-frequency range, without which the results are not reproducible and Eq. (11) cannot be checked.
- Retain the simulation-Preserve the model, parameters and output figures so that measured and simulated behaviour can be compared.

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