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High Speed and Area Efficient Scalable N-bit Digital Comparator

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Abstract

Digital comparators are fundamental components in modern digital systems, playing a crucial role in applications such as arithmetic operations, digital signal processing, pattern recognition, and data compression. Conventional comparator designs often suffer from limitations including high power consumption, increased delay, large area overhead, and sensitivity to clock-related issues. This paper proposes a scalable N-bit digital comparator that optimizes speed, power, and area using a novel Exclusive-OR–NOR (EX-OR-NOR) cell. The proposed architecture minimizes redundant computations and reduces transistor count, thereby improving overall efficiency. Simulation results demonstrate enhanced performance compared to existing comparator designs across operand sizes ranging from 4-bit to 64-bit.

Introduction

A digital comparator is a key combinational circuit used to compare two binary numbers and determine their relational condition (greater than, less than, or equal). It forms the backbone of various applications including built-in self-test (BIST) circuits, signature analyzers, jitter measurement systems, digital image processing, pattern matching, sorting algorithms, and neural networks.

With the increasing demand for high-performance and energy-efficient systems, comparator design has gained significant attention in the field of VLSI design. However, conventional comparator architectures face challenges in achieving optimal trade-offs between speed, power consumption, and silicon area.

Related Work

Several researchers have contributed to the design and optimization of digital comparators, focusing on improving speed, power efficiency, and scalability. The most relevant contributions are summarized below.

Behrooz Parhami proposed counting-based techniques for comparing the Hamming weight of binary vectors. The approach integrates population counting and comparison operations using accumulative and up/down parallel counters. This method achieves improved speed and reduced hardware complexity compared to conventional digital designs, particularly for moderate vector lengths. The efficiency stems from merging counting and comparison into a unified operation, thereby minimizing redundant computations.

Yu Sheng and Weiping Wang addressed the need for efficient comparison of digital image compression algorithms. They developed a component-based comparator system where various compression algorithms are implemented as modular JavaBeans. Communication between components is handled using buffered image class variables. This framework enables flexible and fair comparison of different algorithms while reducing repetitive development effort, making it useful for benchmarking compression techniques.

V. G. Oklobdzija introduced an algorithmic approach for designing a leading zero detector (LZD), which is closely related to comparator logic in arithmetic circuits. The proposed design is modular and scalable, supporting different bit widths efficiently. Implementations in both CMOS and ECL technologies demonstrated superior performance compared to logic synthesis-based designs. Notably, a 64-bit ECL implementation achieved sub-200 ps delay, highlighting the effectiveness of algorithmic design methodologies in high-speed circuits.

Hiroaki Suzuki, Chris H. Kim, and Kaushik Roy proposed a diode-partitioned (DP) domino logic technique to enhance the performance of tag comparators used in cache memory systems. Their design reduces parasitic capacitance and allows the use of smaller keeper circuits in high fan-in gates. Additionally, an improved diode structure boosts NMOS gate voltage, further enhancing speed. The proposed 40-bit comparator demonstrated a 33% delay reduction compared to conventional domino logic circuits in 180 nm CMOS technology.

Saleh Abdel-Hafeez, Ann Gordon-Ross, and Behrooz Parhami presented a high-speed, wide-range comparator based on a scalable parallel prefix structure. The design evaluates bit significance hierarchically, beginning from the most significant bit and proceeding only when necessary. This selective evaluation reduces switching activity and dynamic power consumption. The architecture achieves logarithmic delay performance and maintains consistent fan-in and fan-out irrespective of bit width. Simulation results for a 64-bit comparator showed a delay of 0.86 ns and power dissipation of 7.7 mW using 0.15 µm CMOS technology.

Proposed Plan of Work

The proposed N-bit digital comparator, illustrated in Fig. 4, is designed to efficiently compare two N-bit binary operands. The architecture is divided into two primary modules: the **Comparison Evaluation Module (CEM)** and the **Final Module (FM)**. These modules represent the high-level and low-level operational stages of the comparator, respectively.

The CEM employs a **parallel prefix tree structure** to perform bitwise comparisons between the input operands

$$A = A_{N-1}, A_{N-2}, \ldots, A_0 \text{ and}$$
$$B = B_{N-1}, B_{N-2}, \ldots, B_0.$$

To ensure scalability and regularity for arbitrary bit widths, the operands are partitioned into 4-bit groups (nibbles), such as:

$$A_{N-1}A_{N-2}A_{N-3}A_{N-4}, \ldots, A_3A_2A_1A_0 \text{ and}$$
$$B_{N-1}B_{N-2}B_{N-3}B_{N-4}, \ldots, B_3B_2B_1B_0.$$

This partitioning simplifies hierarchical processing and improves performance for large bit-width comparisons.

1. Hierarchical Set-Based Operation

The comparison process is divided into five sets:

- **Sets 1–4** are part of the **CEM**
- **Set 5** belongs to the **FM**

These sets are organized in a hierarchical prefix manner, where the output of each set feeds into the next stage. The only exception is **Set 1**, whose outputs are simultaneously provided to **Sets 2 and 3**.

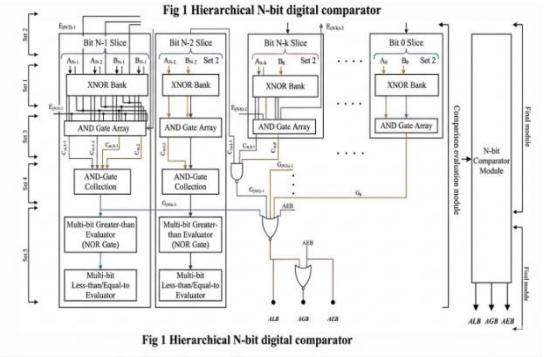


Fig 1 Hierarchical N-bit digital comparator

2. Set 1: Bitwise Comparison using EX–OR–NOR Cell

Set 1 performs bitwise comparison of operands using a novel **EX–OR–NOR cell** (shown in Fig. 5). This cell is implemented using a hybrid of **pass transistor logic** and **CMOS logic**.

Key features of the proposed EX–OR–NOR cell include:

- Uses **7 transistors** (4 PMOS and 3 NMOS), compared to 8 in conventional designs
- Provides both **EX-OR (difference)** and **EX-NOR (equality)** outputs simultaneously
- Ensures **full voltage swing**, overcoming limitations of earlier 6-transistor designs
- Incorporates:
  - **Transistor M5** for full EX-NOR output swing

- **PMOS feedback transistor** to maintain logic stability
- **CMOS boosting logic** for strong EX-OR output

This optimized design avoids the drive strength limitations typically associated with pass transistor logic.

The outputs of this stage are defined as:

- TKT_KTK: Termination (equality) signal → indicates AK=BKA_K = B_KAK=BK
- DKD_KDK: Difference signal → indicates AK≠BKA_K \ne B_KAK=BK

where K∈[0,N−1]K \in [0, N-1]K∈[0,N−1].

3. Set 2: Generation of Equal Flags

Set 2 processes the **termination signals (T_k)** generated in Set 1. The logic cells in this stage combine termination bits within each 4-bit partition (nibble), starting from the most significant bits (MSB).

- AND-type logic gates are used to propagate equality conditions
- Outputs are **equal flags**: E(N/4)−1,E(N/4)−2,...,E0E_{(N/4)-1}, E_{(N/4)-2}, ..., E_0E(N/4)−1,E(N/4)−2,...,E0

These equal flags serve two important purposes:

1. **Control switching activity** in subsequent stages (power optimization)
2. **Generate comparison requests** for further evaluation

A comparison request is generated only if all preceding bits are equal; otherwise, the process is terminated early by propagating logic '0'. This significantly reduces unnecessary computations and improves efficiency.

4. Set 3 and Set 4: Hierarchical Decision Propagation

In Sets 3 and 4, the comparator refines the comparison results by combining:

- Difference signals DKD_KDK
- Equal flags from Set 2

These stages operate hierarchically to determine whether:

- A>BA > BA>B
- A<BA < BA<B

The design ensures that only the necessary bit positions are evaluated, reducing delay and switching power.

5. Set 5: Final Module (FM)

The Final Module consolidates the outputs from the CEM and generates the final comparison results:

- AGB (A Greater than B)
- ALB (A Less than B)
- AEB (A Equal to B)

This stage ensures correct decision generation with minimal logic depth.

6. Key Advantages of Proposed Design

- **Scalability:** Supports arbitrary N-bit inputs
- **Reduced delay:** Parallel prefix structure minimizes critical path
- **Low power consumption:** Controlled switching activity
- **Area efficiency:** Reduced transistor count using optimized EX–OR–NOR cell
- **Improved signal integrity:** Full voltage swing outputs

Circuit Description

The proposed N-bit comparator consists of:

1. Bitwise Comparison Stage

Each pair of input bits is processed using EX-OR-NOR cells to generate equality and difference signals.

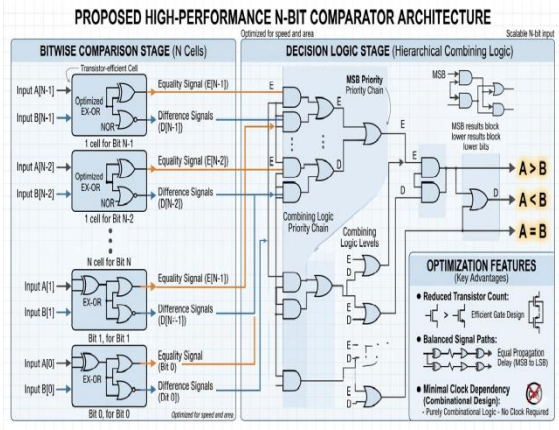
2. Decision Logic Stage

The outputs from the first stage are combined using hierarchical logic to determine:

- A > B
- A < B
- A = B

3. Optimization Features

- Reduced transistor count
- Balanced signal paths
- Minimal clock dependency (combinational design)



Performance Evaluation

1. Metrics Considered

- Propagation Delay
- Power Consumption
- Area (Transistor Count)

2. Results Summary

Simulations were conducted for input sizes ranging from 4-bit to 64-bit. The proposed comparator shows:

- **Reduced delay** compared to ripple and domino-based designs
- **Lower power consumption** due to minimized switching activity
- **Smaller area** due to compact EX-OR-NOR cell design

3. Comparative Analysis

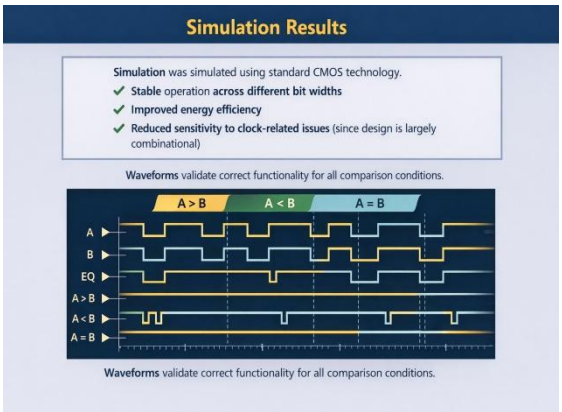
Parameter	Conventional Designs	Proposed Design
Speed	Moderate	High
Power	High	Low
Area	Large	Compact
Scalability	Limited	High

6. Simulation Results

The design was simulated using standard CMOS technology. Results confirm:

- Stable operation across different bit widths
- Improved energy efficiency
- Reduced sensitivity to clock-related issues (since design is largely combinational)

Waveforms validate correct functionality for all comparison conditions.



Conclusion

This paper presents a high-speed, area-efficient scalable N-bit digital comparator using a novel EX-OR-NOR cell. The proposed design overcomes major limitations of existing comparator architectures, including high power consumption, large area, and delay inefficiencies. The modular and scalable nature of the design makes it suitable for a wide range of applications in modern VLSI systems.

Future work may include implementation in advanced technology nodes and integration into complex digital systems.

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