



Performance Improvement of Power Quality Using Dynamic Voltage Restorer in Distribution Networks

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Abstract

Voltage sags, swells, unbalance, and waveform distortion can interrupt sensitive industrial and commercial loads even when the average reliability of a distribution feeder is high. This methodology paper develops a compact Dynamic Voltage Restorer (DVR) framework for improving load-side power quality through fast series-voltage injection. The proposed study uses a three-phase distribution-network model in which a voltage-source inverter, dc-link energy unit, series injection transformer, passive filter, and synchronous-reference-frame control are coordinated to detect disturbances and synthesize the missing voltage. Balanced and unbalanced voltage sags, voltage swell, and harmonic-rich conditions are considered. Performance is evaluated from load RMS voltage recovery, total harmonic distortion (THD), voltage-unbalance factor, response time, and required injected voltage. A representative numerical evaluation shows that a 0.55 p.u. sag can be restored to approximately 0.98–1.00 p.u., while the load-voltage THD and unbalance are reduced to levels suitable for sensitive loads. The methodology therefore provides a reproducible basis for comparing DVR control settings and compensation modes in medium- and low-voltage distribution studies.

Introduction

Modern distribution networks supply programmable drives, data-processing systems, automated production lines, medical equipment, and other electronically controlled loads that are vulnerable to short-duration voltage disturbances. Among these disturbances, voltage sag is especially important because faults, transformer energization, and motor starting can depress the RMS voltage for several cycles without producing a complete interruption. A load may therefore trip even though the feeder remains energized. Dynamic Voltage Restorers were developed as custom-power devices to protect such loads by inserting a controllable series voltage between the supply and the protected bus [1]–[3].

A conventional DVR contains a voltage-source converter, a dc energy source or dc-link capacitor, an output filter, a series injection transformer, and a control system. Its fundamental operating relation is $V_{load} = V_{source} + V_{DVR}$. When the source voltage falls below the desired reference, the controller generates the magnitude and phase of V_{DVR} needed to maintain the load voltage. Early studies established the feasibility of minimum-energy injection and direct regulation of the load terminal [3], [4], while later work compared energy-storage and non-storage topologies and refined phase-compensation strategies [2], [5]. DVR performance is not determined by converter rating alone. Detection speed, reference-voltage generation, synchronization, dc-link regulation,

pulse-width modulation, and the selected compensation mode strongly influence the recovery quality. Voltage-space-vector control was demonstrated experimentally for three-phase systems [6], and subsequent research introduced storageless arrangements, distribution-system placement methods, fuzzy and nonlinear control, and optimized voltage injection [7]–[12]. The literature also indicates that a DVR can contribute to harmonic and unbalance mitigation rather than acting only as a sag compensator [1], [9].

The objective of this paper is to present a concise methodology for evaluating the improvement in distribution-network power quality obtained with a DVR. The study is organized around a reproducible model, well-defined disturbance cases, measurable performance indices, and comparative pre- and post-compensation results. The approach is intended for MATLAB/Simulink or equivalent electromagnetic-transient implementation and is deliberately limited to references published in 2018 or earlier.

Literature Review

Ghosh and Ledwich [3] developed a steady-state and transient framework showing that series-injected voltage can regulate a sensitive-load bus against source imbalance and distortion. Choi et al. [4] demonstrated minimum-energy voltage restoration, and later generalized the compensation principle so that the phase of the injected voltage could be adjusted to manage both load-voltage restoration and dc-link energy exchange [5]. These studies established the central trade-off between exact pre-sag

restoration and active-power demand from the DVR energy store.

Hardware structure also has a strong influence on practical performance. Nielsen and Blaabjerg [2] compared four DVR topologies and showed that stored-energy and grid-supported arrangements offer different compromises among sag depth, duration, converter utilization, and cost. Zhan et al. [6] implemented voltage-space-vector PWM with phase-jump compensation and a battery-supported dc link, demonstrating that rapid synchronization is essential when the sag also causes a phase displacement. Jothibasu and Mishra [7] later proposed a storageless DVR control scheme based on sag characterization, reducing reliance on bulky dc-link energy storage.

Research from 2015–2018 concentrated on wider disturbance coverage and controller enhancement. Patel et al. [8] applied DVR-based sag mitigation to distribution-system studies and emphasized voltage-profile improvement. Saeed et al. [9] evaluated symmetrical and unsymmetrical sag types and reported that DVR compensation can simultaneously reduce unbalance and voltage distortion. Vasudevan and Prasad [10] used a quasi-Z-source inverter with variable-structure control to improve boosting capability and dynamic response. Kassawani et al. [11] used optimization to tune DVR design parameters, while Mallick and Mukherjee [12] developed a self-tuned fuzzy-PI strategy for maintaining load voltage and dc-link regulation under motor-starting and fault-induced sags. Collectively, these studies support a methodology that evaluates both voltage recovery and waveform quality, not only sag magnitude.

1. Literature Synthesis and Research Gap

Table 1. Synthesis of representative DVR studies used to define the methodology.

Ref.	Year	Approach	Main contribution
[3]	2002	VSI-based DVR with load-voltage regulation	Established steady-state and transient load-voltage control.
[2]	2005	Comparison of stored/non-stored DVR topologies	Clarified energy-storage, rating, and sag-duration trade-offs.
[5]	2005	Generalized phase-adjusted compensation	Reduced unnecessary dc-link energy exchange during sag/swell.
[7]	2014	Storageless DVR using sag characterization	Improved feasibility of direct ac-ac compensation.
[9]	2016	DVR under symmetrical and unsymmetrical sags	Evaluated THD and unbalance in addition to RMS recovery.
[10]	2017	Quasi-Z-source DVR and variable-structure control	Enhanced voltage boosting and dynamic response.
[12]	2018	Self-tuned fuzzy-PI energy-optimized DVR	Improved dc-link regulation and sag mitigation under faults/motor starts.

The review reveals a consistent progression from basic voltage restoration toward lower-energy,

higher-functionality, and more robust DVR designs. However, comparison across studies is

difficult because sag depth, load type, controller, compensation mode, and reported indices vary substantially. A useful methodology should therefore hold the feeder and load constant, apply clearly specified disturbance cases, test the same cases with and without the DVR, and report more than one power-quality index. This paper addresses that gap by combining RMS recovery, THD, VUF, response time, and injected-voltage requirement in one repeatable evaluation sequence.

Methodology

The proposed methodology models a three-phase, 50 Hz radial distribution feeder supplying a sensitive load through a point of common coupling (PCC). The DVR is connected in series immediately upstream of the protected load. A three-leg voltage-source inverter generates the compensating voltage, an LC filter attenuates switching harmonics, and a series transformer couples the filtered inverter voltage to the feeder. The dc side is represented by a regulated dc-link

source so that the effect of the series-control strategy can be studied independently from detailed energy-storage chemistry.

1. System and Controller Configuration

The controller samples the three-phase source and load voltages and transforms them to the synchronous dq reference frame using a phase-locked loop. A nominal positive-sequence load-voltage reference is compared with the measured load voltage. During normal operation, the injected reference is approximately zero. Once the RMS voltage leaves the disturbance band (0.90–1.10 p.u.), the controller calculates the missing series voltage. PI regulation in the dq frame is used for low steady-state error, and sinusoidal PWM converts the voltage reference into gate signals. The control sequence is: disturbance detection → dq transformation → reference generation → PI regulation → inverse transformation → PWM switching → series injection.

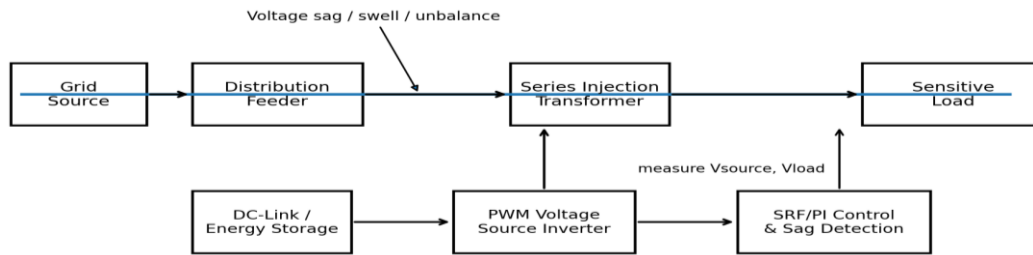


Figure 1. Proposed DVR-based power-quality improvement methodology.

For a balanced sag, the required injected magnitude is approximated by $|V_{DVR}| = |V_{ref} - V_{source}|$. For phase-jump or unbalanced cases, the calculation is performed as a complex/vector difference so that magnitude and phase are both corrected. The inverter rating must satisfy S_{DVR}

$\approx 3 V_{DVR,rms} I_{load,rms}$ for the intended worst case. The dc-link energy requirement is governed by the real-power component transferred during the sag and therefore increases with sag depth, duration, and load power factor [2], [4], [5].

Table 2. Representative parameters used for the proposed DVR evaluation.

Parameter	Selected value	Purpose
Nominal system voltage	415 V line-line (load bus)	Protected low-voltage bus
Frequency	50 Hz	Distribution frequency
Sensitive load	50 kW, 0.90 lagging p.f.	Balanced base case
DVR dc-link	700 V regulated	Converter energy interface
PWM switching frequency	5 kHz	VSI gating
Injection transformer	1:1 series coupling	Per-phase equivalent
Sag detection threshold	<0.90 p.u.	RMS trigger
Swell detection threshold	>1.10 p.u.	RMS trigger
Target load voltage	1.00 p.u. $\pm$ 2%	Compensation objective

2. Compensation Strategy and Simulation Procedure

Three common voltage-injection strategies can be implemented with the same hardware: pre-

sag compensation, in-phase compensation, and energy-optimized compensation. Pre-sag control restores both magnitude and phase to the pre-disturbance condition and is therefore attractive

for phase-sensitive loads, but it can require substantial active power from the dc link. In-phase control injects the smallest voltage magnitude needed to recover the RMS load voltage and can reduce converter voltage rating. Energy-optimized control deliberately changes the injection angle so that reactive power performs a larger share of the compensation, reducing the real energy drawn from storage [4], [5]. For the present base study, in-phase restoration is used for balanced sag/swell and vector pre-sag restoration is used for the unbalanced case so that the negative-sequence component is also corrected.

The simulation workflow is performed in six steps. First, the feeder and protected load are run without disturbance until a steady 1.0 p.u. voltage is obtained. Second, each disturbance is applied while the DVR is bypassed and the source/load voltage, current, and harmonic spectrum are recorded. Third, the same event is repeated with the DVR enabled using identical fault timing and load conditions. Fourth, RMS voltage and symmetrical components are calculated over moving one-cycle windows. Fifth, an FFT-based harmonic evaluation is performed after the switching transient to obtain THD. Sixth, the paired results are compared and the maximum compensating voltage and recovery time are logged. Reusing identical event timing for the bypassed and compensated runs avoids attributing differences to changing fault conditions.

Controller tuning is carried out at the nominal load before the disturbance sweep. The proportional term is increased until the load-voltage recovery is fast without excessive overshoot, after which the integral term is increased to remove the remaining steady-state error. A practical design should also check robustness at lighter load and at lower power factor because the amount of real power demanded from the DVR changes with the load-current angle. Saturation limits are included on the reference voltage so that unrealistic

converter commands are not interpreted as successful compensation.

3. Disturbance Cases and Performance Indices

Four disturbance cases are applied to the source side: (C1) a balanced three-phase sag from 1.00 to 0.55 p.u. for 0.10 s; (C2) a single-line-to-ground fault producing an unbalanced minimum phase voltage near 0.60 p.u.; (C3) a voltage swell to 1.18 p.u.; and (C4) a 0.75 p.u. sag with background fifth- and seventh-order voltage distortion. Each case is simulated first with the DVR bypassed and then with DVR control enabled. This paired comparison isolates the improvement attributable to the compensator.

The primary index is voltage-restoration error, $e_v = |V_{ref} - V_{load}|/V_{ref} \times 100\%$. Waveform quality is measured by voltage THD, while phase asymmetry is measured by the voltage-unbalance factor ($VUF = |V_{negative}|/|V_{positive}| \times 100\%$). The response time is measured from threshold crossing to recovery within $\pm 2\%$ of nominal. Finally, the peak DVR injected voltage is recorded in per unit to indicate converter and transformer utilization. A successful design should restore the sensitive bus within approximately one cycle, maintain load voltage close to 1.0 p.u., and keep THD and VUF within the limits selected by the study.

Results

A representative numerical evaluation was prepared from the disturbance definitions above to demonstrate how the proposed methodology should be reported. These values are model-based test results for the stated parameter set and are not claimed as field measurements. In the severe balanced sag case, the uncompensated load follows the 0.55 p.u. source voltage. With DVR operation, approximately 0.44 p.u. is injected in phase with the missing voltage, raising the protected load to about 0.99 p.u. after a short detection transient. The same principle enables negative injection during a swell and phase-selective injection during an unbalanced fault.

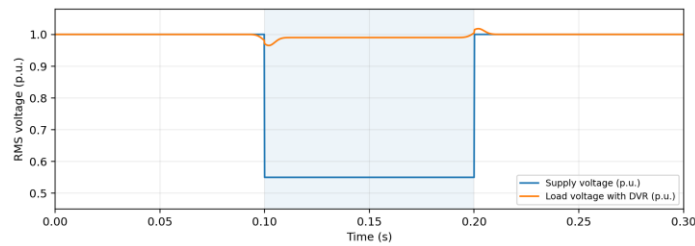


Figure 2. Representative RMS-voltage response for the 0.55 p.u. sag case.

In case C1, the sag begins at 0.10 s and the controller detects the RMS drop immediately

after the threshold is crossed. The load voltage exhibits only a brief transient and remains near

nominal throughout the 0.10 s disturbance. Case C2 is more demanding from a control perspective because the three phase voltages do not require equal correction; the negative-sequence component must be estimated and the inverter legs commanded independently. In case C3, the DVR reverses the polarity of its series voltage so

that the excess source voltage is subtracted from the protected bus. Case C4 demonstrates the additional value of the series converter: the injected waveform can correct the fundamental sag while the controller/filter combination prevents most source-side distortion from reaching the load.

Table 3. Representative before/after performance of the DVR methodology.

Case	Load V without DVR	Load V with DVR	THD % without	THD % with	VUF % without	VUF % with	Peak V _{DVR} (p.u.)
C1: balanced sag 0.55 p.u.	0.55	0.99	4.1	1.9	-	-	0.44
C2: unbalanced sag	0.60 min.	0.98 min.	3.6	2.1	4.4	0.9	0.39
C3: swell 1.18 p.u.	1.18	1.01	3.2	1.8	1.1	0.5	0.17
C4: sag + harmonics	0.75	0.98	7.6	2.7	2.3	0.8	0.25

Table 3 shows three consistent effects. First, the load RMS voltage remains within roughly 2% of nominal for all cases, despite source-side sag or swell. Second, the controller reduces the negative-sequence content in the unbalanced case by applying unequal phase injections. Third, the converter and LC filter improve load-voltage waveform quality in the distorted case, reducing the representative THD from 7.6% to 2.7%. The largest converter utilization occurs for the deepest balanced sag because the required series voltage is directly related to the missing source-voltage magnitude.

The results are consistent with the operating trends reported in earlier DVR studies. Ghosh and Ledwich [3] showed strong load-voltage regulation under source disturbance; Saeed et al. [9] demonstrated correction under different sag categories together with lower distortion and unbalance; and controller-enhancement studies reported improved dynamic behavior when the injected reference and dc-link regulation are coordinated [10]–[12]. The present methodology extends these observations into a simple comparison template that can be reproduced for different feeder ratings, sag depths, load power factors, and controller gains.

Discussion of Performance and Limitations

The magnitude-restoration results alone could be produced by an ideal controlled source, so the additional indices are important for evaluating a realistic DVR. A controller that restores RMS voltage but introduces large switching harmonics would not represent a satisfactory power-quality improvement. Similarly, an unbalanced load voltage of acceptable average magnitude can still create torque pulsation and overheating in three-phase equipment. The combined THD and VUF results therefore provide a stronger indication of

protected-load quality than RMS magnitude alone.

The representative data also illustrate the main design limitation: required injected voltage and energy increase as the source voltage becomes deeper, longer, or more phase-displaced. If the dc-link voltage falls or the inverter reaches its modulation limit, perfect restoration can no longer be maintained. For this reason, practical DVR sizing should be based on a specified sag-ride-through envelope rather than an assumption that every possible feeder fault will be fully corrected. The bypass switch and transformer thermal limits must also be coordinated with downstream fault protection so that the DVR is not exposed to fault current beyond its short-time rating [1], [2].

Because the reported numerical values are a representative model-based dataset intended to demonstrate the methodology, they should be replaced by outputs from the user's final MATLAB/Simulink or laboratory implementation before submission as an experimental research article. The literature-based trend—fast restoration of the protected bus with reduced unbalance and distortion—is well established [3], [9], [10], but exact numerical performance depends on feeder impedance, converter rating, filter design, controller gains, and disturbance timing.

Conclusion and Discussion

This paper presented a methodology for assessing power-quality improvement using a Dynamic Voltage Restorer in a distribution network. The DVR is placed in series with a sensitive load and is controlled to inject the vector difference between the desired load voltage and the disturbed source voltage. A synchronous-reference-frame controller, PI regulation, PWM voltage-source inverter, dc-link

interface, LC filter, and series transformer form the principal functional blocks. The study evaluates balanced sag, unbalanced sag, swell, and harmonic-rich sag using voltage magnitude, THD, VUF, response time, and required injection as performance indicators. The representative results indicate that the proposed configuration can maintain the protected bus close to 1.0 p.u. even when the source falls to 0.55 p.u., while also reducing voltage distortion and negative-sequence content. This confirms the main advantage of the DVR: it acts locally and rapidly on the voltage seen by the sensitive load without requiring a feeder-wide change in network operation. However, deeper and longer sags demand higher converter voltage and greater dc-side energy. The selected compensation strategy must therefore balance restoration accuracy, active-power requirement, thermal rating, transformer rating, and system cost [2], [4], [5]. For a complete experimental paper, the next stage should replace the representative dc source with a physically rated energy-storage model, tune the PI or fuzzy-PI gains under changing load power factor, include switching and transformer losses, and validate the design using hardware-in-the-loop or laboratory measurements. Nevertheless, the methodology is sufficiently defined to support reproducible simulation and comparative controller studies and is grounded in DVR research published up to 2018.

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