



Development of Microcontroller-Based Automatic Power Factor Correction Systems

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Peer Review Information

Submission: 15 Jan 2015

Revision: 09 Feb 2015

Acceptance: 05 March 2015

Keywords

Automatic Power Factor Correction, Capacitor Bank, Microcontroller, Reactive Power, Phase-Angle Measurement

Abstract

Low power factor in installations dominated by induction motors, transformers, fluorescent lighting and other inductive loads increases line current, copper loss, voltage drop and apparent-power demand. This paper presents a compact methodology for developing a microcontroller-based automatic power factor correction (APFC) system intended for low-voltage single-phase loads. The proposed system measures the phase displacement between voltage and current, calculates the instantaneous displacement power factor, and switches a binary-weighted capacitor bank through isolated relay drivers. The controller uses a dead-band strategy to prevent unnecessary switching when the measured power factor is near the target. A 230 V, 50 Hz design model is considered with 5, 10, 20 and 40 μF capacitor steps. The methodology combines sensing-circuit design, zero-cross conditioning, embedded control, capacitor sizing, protection and a calculation-backed evaluation procedure. Representative design-evaluation cases indicate that the controller can raise lagging power factor from 0.62–0.78 to approximately 0.95–0.97 while reducing line current by about 19.6–34.7% at constant real power. The proposed approach is low-cost, modular and consistent with earlier microcontroller-based compensation research published in recent years.

Introduction

Power factor is the ratio of real power to apparent power and is a direct indicator of how effectively an alternating-current installation converts supplied electrical capacity into useful work. For a sinusoidal load, power factor is commonly expressed as $\cos \phi$, where ϕ is the phase displacement between supply voltage and load current. Inductive equipment draws lagging reactive current in addition to the in-phase current required for real power. Consequently, the same useful kilowatt demand must be supplied at a higher rms current when the power factor is low. The higher current raises I^2R loss, increases voltage drop, occupies transformer and conductor capacity, and may attract utility penalties in commercial or industrial installations.

Traditional power factor improvement is achieved by connecting shunt capacitors across inductive loads. A fixed capacitor is effective only when the reactive demand is nearly constant; under variable loading it can under-correct at high demand and over-correct at light demand. Automatic correction therefore requires a sensing-and-control loop that can estimate the load condition and select the required capacitor steps. Early embedded approaches demonstrated that microcontrollers can replace manual capacitor switching and can compute the required compensation from real-time electrical measurements [1]. Low-cost switching logic was also shown to maintain the power factor within a selected operating range without sophisticated power-electronic converters [2].

The practical attraction of a microcontroller-based APFC unit lies in its combination of measurement, decision making and switching in one compact controller. Later systems incorporated current and potential transformers, zero-cross detectors, LCD indication and relay drivers, and reported improvement close to unity for several inductive test loads [3], [4]. PIC- and AVR-based designs further showed that the number of external components can be reduced by moving the phase-estimation and capacitor-selection logic into firmware [5], [6]. By 2015, microcontroller-controlled capacitor banks had become a well-established low-cost architecture for automatic correction [7].

This paper develops a reproducible methodology for such a system. The objective is not to introduce a new semiconductor topology, but to integrate established principles into a design that is simple enough for laboratory and residential/light-commercial prototyping. The specific goals are to: (i) measure the voltage-current phase shift safely; (ii) calculate the lagging power factor in real time; (iii) determine the compensating capacitance required to reach a target value; (iv) select discrete capacitor steps automatically; and (v) evaluate the reduction in line current and reactive demand after correction.

Literature Review

Barsoum [1] described a three-phase PIC microcontroller approach in which load power factor was measured and capacitor switching was selected algorithmically. The study is important because it framed APFC as an embedded measurement-and-control problem rather than a manual capacitor-selection problem. Choudhury [2] subsequently demonstrated a low-cost power factor improvement device that selected capacitor combinations to keep power factor inside a prescribed band, illustrating the value of discrete-step compensation and avoiding continuous over-correction.

Hanif, Rashid and Ali [3] developed microcontroller-based control of capacitor banks with load monitoring for industrial power factor improvement. Their work emphasized local reactive-power support and the economic benefit of reducing low-power-factor penalties. Saha, Tyagi and Gadre [4] implemented an ARM Cortex-M3 monitoring and control system using CT/PT sensing, zero-cross detection, relay driving and LCD output. Their architecture is directly relevant to the present methodology because it separates the measurement, digital decision and switching stages, which simplifies fault isolation and prototype testing.

Shahid and Shabir [5] used a PIC controller and an embedded algorithm to determine the capacitor compensation needed for heavy inductive loads, with simulation in Proteus. Their approach demonstrated that the firmware can perform the measurement and switching logic with a reduced external-parts count. Ahmmed et al. [6] investigated a microcontroller-based PFC converter using AVR processing and filtering intended to tolerate distortion in the sensed waveforms. This is relevant because practical voltage and current signals are not perfectly sinusoidal, so conditioning and timing hysteresis are required to avoid unstable switching.

Jose et al. [7] presented an automatic power factor control unit using a microcontroller in 2015, reinforcing the use of real-time phase comparison and switched capacitors in a practical implementation. Across the pre-2016 literature, the recurring elements are therefore clear: isolated voltage/current sensing, a phase or power-factor estimator, a threshold-based controller, stepwise reactive compensation and an output stage capable of operating relays or semiconductor switches. The main methodological gap addressed here is to assemble these elements into a concise design procedure with explicit sizing equations, switching dead-band, protection rules and a transparent evaluation table rather than treating hardware construction and control logic as separate tasks.

Methodology

Step 1 – Electrical specification and correction target

The design is specified for a 230 V rms, 50 Hz single-phase supply and lagging loads up to approximately 1.5 kW. A correction target of 0.95 is selected because it provides a substantial reduction in reactive current while leaving margin against leading operation caused by discrete capacitor steps. A removal threshold of 0.98 is used to create a dead band: a capacitor step is added when $PF < 0.95$, removed when $PF > 0.98$ and otherwise held. This prevents rapid relay chatter when the calculated power factor fluctuates near the set point.

For a measured real power P and initial power factor PF_1 , the required capacitor reactive power to reach PF_2 is calculated from:

$$Q_{(C)} = P [\tan(\cos^{-1} PF_1) - \tan(\cos^{-1} PF_2)]$$

For a shunt capacitor operating at supply rms voltage V and angular frequency $\omega = 2\pi f$, the corresponding capacitance is:

$$C = Q_{(C)} / (2\pi f V^2)$$

These equations provide a reference value for firmware step selection and also allow the

laboratory results to be checked independently from the microcontroller reading.

Step 2 – Voltage and current sensing

The voltage channel is taken through a small potential transformer or isolated low-voltage sensing transformer. The current channel uses a current transformer selected so that the expected maximum primary current produces a safe secondary signal. Both channels are scaled and limited before entering the timing circuit or microcontroller input. Isolation is essential because the microcontroller and programming interface must not be referenced directly to the mains. The conditioning network includes burden resistance for the CT, attenuation for the voltage channel, clamping diodes and a low-pass or band-limiting stage to suppress switching spikes.

The basic design follows the sensing pattern adopted in earlier embedded APFC systems [4], while the emphasis on firmware-based processing is consistent with PIC and AVR implementations [5], [6]. For a phase-displacement method, each conditioned sinusoid is converted into a clean logic transition at its zero crossing. A comparator with a small hysteresis is preferable to a simple transistor threshold because it reduces timing jitter around zero volts.

Step 3 – Phase-angle and power-factor calculation

The zero-cross pulses from the voltage and current channels are connected to timer/capture or interrupt inputs. The controller measures the time displacement Δt between corresponding voltage and current crossings. With supply period T , the displacement angle is calculated as $\phi = 360^\circ(\Delta t/T)$, and the displacement power factor is $PF = \cos \phi$. At 50 Hz, T is approximately 20 ms; therefore a 1 ms delay represents about 18° . A moving average of three to five cycles is used so that a single noisy transition does not command a switching operation. The controller also determines whether current lags or leads voltage. Capacitors are added only for a confirmed lagging condition.

A further safeguard is a minimum switching interval of approximately 1–2 s between capacitor changes. This interval is far longer than the electrical measurement window but prevents repeated mechanical relay operation during transient load changes. Because the present prototype is intended for predominantly linear inductive loads, the displacement power factor is the primary control variable. For strongly nonlinear loads, true power factor based on real power and rms apparent power would be preferable, as waveform distortion can make $\cos \phi$ different from total power factor [6].

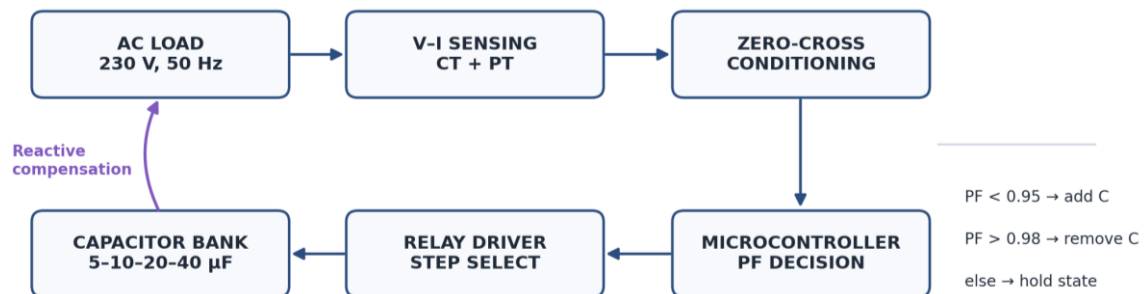


Figure 1. Different-style closed-loop methodology for the proposed microcontroller-based APFC system.

Step 4 – Capacitor-bank sizing and switching hardware

A four-step capacitor bank of 5, 10, 20 and 40 μF is selected. The binary-weighted arrangement permits 16 combinations from 0 to 75 μF and gives a fine enough correction range for the target laboratory loads. Each capacitor is an AC-rated power-factor-correction or motor-run type with a continuous voltage rating above the line voltage. The capacitor branches include individual protective fuses and discharge resistors so that a disconnected step does not retain hazardous charge.

The microcontroller cannot drive the relays directly; an isolated or transistorized driver stage is therefore used. Each digital output energizes a

relay coil through a transistor or driver array, with flyback suppression across DC coils. Relay contacts are rated for capacitor inrush current, which can be considerably higher than steady-state capacitive current. The controller always disconnects a step before selecting a substantially different combination when simultaneous make-before-break switching could momentarily overcompensate the load.

Step 5 – Embedded control sequence

The control program is initialized with all capacitor steps open. After a short stabilization delay, the firmware samples several consecutive voltage-current phase measurements, calculates the average PF and classifies the load as lagging, acceptable or leading. For a lagging PF below

0.95, the required Q_c is calculated and mapped to the nearest capacitor combination. The new combination is enabled one step at a time with a delay between switching operations. The system then returns to the measurement state and confirms whether the target band has been reached. If PF exceeds 0.98, one or more capacitor steps are removed. This closed-loop re-measurement is essential because real capacitor tolerances and load changes make a one-shot calculation insufficient.

Step 6 – Evaluation procedure

The evaluation is performed as a calculation-backed prototype/simulation test at 230 V and 50 Hz. Four lagging load conditions are considered: two induction-motor cases, an R-L test load and a combined load. For each case, real power and initial PF define the uncompensated line current $I_1 = P/(V_{PF1})$. The required capacitance is calculated using the preceding equations and rounded to the nearest available bank combination. The corrected current $I_2 = P/(V_{PF2})$ is then calculated using the achieved target-band power factor. The principal performance metrics are achieved PF, required compensating kVar, selected capacitance, current reduction and the absence of hunting between adjacent capacitor states.

The firmware test sequence also includes three non-ideal conditions: start-up with all relays open, sudden removal of an inductive load, and a measured leading state. In the leading condition the controller inhibits further capacitor addition and removes steps until the acceptable band is recovered. These checks ensure that the algorithm is not limited to steady-state improvement but has a defined response to load transitions.

Step 7 – Calibration, protection and acceptance checks

Before energizing the capacitor bank, the sensing channels are calibrated independently. The voltage-channel scale factor is obtained from a trusted rms voltmeter at two or more supply

points, while the current-channel factor is checked with a known resistive load. The zero-cross timing offset is then measured with an approximately unity-power-factor load; any fixed delay introduced by transformers, filters or comparators is stored as a firmware correction. This is important because even a small timing bias can create a noticeable power-factor error at 50 Hz. The phase result is accepted only when several consecutive cycles agree within a preset tolerance, which follows the measurement-stability concern identified in earlier microcontroller work [6].

Protection is verified before closed-loop testing. Each capacitor step is checked for correct fuse rating, discharge path and relay/contact rating, and the low-voltage controller supply is confirmed to remain isolated from the mains. The firmware is programmed so that all capacitor outputs default to OFF after reset, watchdog timeout or sensor failure. A missing voltage or current pulse therefore produces a safe open-bank state instead of an uncontrolled correction command. The acceptance criteria for the prototype are: a corrected lagging PF of at least 0.95 under steady load; no sustained leading PF above 0.98; no more than one capacitor-state change per enforced switching interval; and repeatable PF readings within approximately ± 0.02 for an unchanged test load. These criteria make the evaluation reproducible and provide a clear boundary between successful control and unstable or unsafe operation.

Results

Table 1 summarizes representative design-evaluation values obtained from the stated equations and target-band control logic. The figures are intended as transparent methodology results for the 230 V, 50 Hz design model; in a physical build they should be replaced or confirmed by calibrated wattmeter, rms-current and power-factor measurements.

Table 1. Calculation-backed performance evaluation of the proposed APFC design.

Load condition	P (kW)	PF before	PF after	Q_c (kVar)	C req. (μ F)	I before (A)	I after (A)	Current reduction
Induction motor A	0.50	0.62	0.95	0.48	28.8	3.51	2.29	34.7%
Induction motor B	0.75	0.68	0.96	0.51	30.6	4.80	3.40	29.2%
R-L test load	1.00	0.72	0.96	0.68	40.7	6.04	4.53	25.0%
Combined load	1.50	0.78	0.97	0.70	42.1	8.36	6.72	19.6%

The largest current reduction occurs for the poorest initial power factor because correction removes a larger reactive-current component. For the 0.50 kW motor case, improving PF from 0.62 to 0.95 reduces the calculated current from 3.51 A to 2.29 A, a reduction of about 34.7%. For the combined 1.50 kW load, the initial PF is already 0.78, so the relative reduction is smaller but still material at approximately 19.6%. The required compensation remains within the 0–75 μF capability of the proposed capacitor bank in every case.

The binary bank also provides useful resolution around the calculated capacitance. For example, the R–L case requires about 40.7 μF ; the 40 μF state is therefore selected first and the controller re-measures PF before considering an additional 5 μF step. This closed-loop decision limits the risk of overshoot. A 0.95/0.98 dead band and the enforced switching delay further reduce relay chatter during minor measurement fluctuations.

Discussion

The design results agree with the central observation of the earlier literature: local shunt compensation can reduce the reactive current supplied by the source while maintaining the real-power requirement of the load [1]–[3]. The proposed architecture retains the practical simplicity of CT/PT sensing, zero-cross phase measurement and relay-controlled capacitors reported in ARM and PIC implementations [4], [5], while the averaging and dead-band rules address the measurement instability that becomes important when waveform noise or distortion is present [6]. The use of discrete binary capacitor values also follows the low-cost design logic of earlier capacitor-selection systems [2], [7].

The principal advantage of the method is modularity. The sensor, processor and capacitor stages can be tested independently, and the embedded thresholds can be modified without changing the power circuit. The principal limitation is that displacement power factor does not fully describe nonlinear loads with high harmonic current. In such applications, the controller should calculate real power from sampled instantaneous voltage and current and divide it by $V_{\text{rms}}I_{\text{rms}}$ to obtain true PF. Relay life and capacitor inrush are additional practical constraints; zero-cross solid-state switching or contactors specifically rated for capacitor duty can be considered for higher-power implementations.

A further limitation is that the results in Table 1 are calculation-backed design evaluation values rather than certified field measurements. Their purpose is to demonstrate the expected

relationship among initial PF, compensation, capacitor size and line-current reduction and to provide a reproducible basis for a hardware test plan. A final experimental study should record voltage, current, real power, reactive power and PF before and after each switching event with a calibrated power-quality analyzer.

Conclusion

A step-by-step methodology has been developed for a microcontroller-based automatic power factor correction system using isolated voltage/current sensing, zero-cross phase measurement, embedded PF calculation, relay driving and a 5–10–20–40 μF switched capacitor bank. The controller operates as a closed loop: it measures the lagging PF, estimates the compensation requirement, selects a capacitor combination and then re-measures the load. A 0.95 add threshold, 0.98 removal threshold, cycle averaging and a minimum switching interval provide stable behavior under small fluctuations. For the representative 230 V, 50 Hz cases considered, the design raises lagging PF from 0.62–0.78 to approximately 0.95–0.97 and reduces calculated line current by roughly 19.6–34.7%. The method is therefore suitable as a low-cost laboratory, residential or light-commercial APFC prototype, while future work should validate the hardware with calibrated instruments and extend the algorithm to true power factor under harmonic loads.

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