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Recent Advances in Deep Learning-based Area Efficient 1024-Point Pipelined Radix-4 FFT Processor for Biomedical Application: A Systematic Review

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Abstract

Fast Fourier Transform (FFT) plays a crucial role in biomedical signal processing, including electroencephalography (EEG), electrocardiography (ECG), and medical imaging applications. The increasing demand for real-time, low-power, and high-throughput processing has driven the development of optimized FFT architectures, particularly the 1024-point pipelined Radix-4 FFT processor. Recent advancements integrate deep learning techniques with FFT-based architectures to enhance feature extraction, noise reduction, and computational efficiency in biomedical systems. This review presents a comprehensive analysis of recent developments in deep learning-assisted FFT processors, focusing on area efficiency, power consumption, and processing speed. Modern architectures emphasize pipelined and parallel processing to achieve high throughput while minimizing hardware complexity. Additionally, hybrid approaches combining convolutional neural networks (CNNs) with FFT have demonstrated improved performance in biomedical signal analysis, including enhanced accuracy in classification and diagnosis. Furthermore, emerging low-power FFT designs such as minimal architecture single-delay feedback (mSDF) structures show significant reductions in power consumption, making them suitable for wearable and implantable medical devices. This systematic review highlights key advancements, identifies research gaps, and discusses future directions in designing efficient FFT processors integrated with deep learning for biomedical applications.

Introduction

The Fast Fourier Transform (FFT) is a fundamental algorithm in digital signal processing (DSP), widely used to convert signals from the time domain to the frequency domain with significantly reduced computational complexity. Compared to the direct Discrete Fourier Transform (DFT), FFT reduces computational complexity from $O(N^2)$to $O(N\log N)$, making it highly efficient for large-scale signal processing applications. In biomedical applications, FFT plays a critical role in analysing physiological signals such as EEG, ECG, and MRI data. These signals are often noisy and require high-resolution spectral analysis, which demands efficient and high-speed FFT processors. The emergence of 1024-point FFT architectures enables detailed frequency-domain analysis, essential for accurate disease diagnosis and monitoring.

Among various FFT algorithms, the Radix-4 FFT is widely preferred due to its reduced number of arithmetic operations compared to Radix-2, leading to improved computational efficiency. Additionally, pipelined architectures enhance throughput by allowing continuous data processing, making them suitable for real-time biomedical systems. However, these benefits come with challenges such as increased hardware complexity, power consumption, and area requirements. Recent advancements in deep learning have significantly influenced FFT-based systems. Deep learning models, particularly convolutional neural networks (CNNs), have been integrated with FFT frameworks to improve signal feature extraction and classification performance.

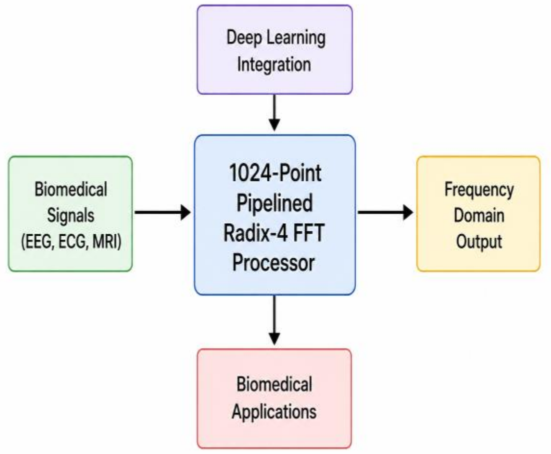

Figure 1. Deep Learning-Based Radix-4 FFT Framework for Biomedical Signal Processing

For instance, FFT-based deep feature learning methods have demonstrated effectiveness in EEG signal classification by transforming signals into frequency-domain representations for neural network processing.
Moreover, hardware-level optimizations such as parallel prefix adders and optimized multipliers have been proposed to enhance FFT processor performance in terms of speed, power, and area efficiency. Advanced architectures like Split-Radix and hybrid FFT designs further improve performance metrics by reducing computational overhead. In biomedical systems, power efficiency is a critical factor, especially for wearable and implantable devices. Recent research has focused on ultra-low-power FFT architectures, such as minimal single-delay feedback (mSDF) designs, which significantly reduce energy consumption while maintaining processing accuracy.
Furthermore, FFT-based deep learning approaches have been applied in medical imaging and genomic signal processing, improving accuracy and reducing noise. These hybrid approaches combine signal processing efficiency with intelligent learning capabilities, enabling advanced diagnostic systems. This paper presents a systematic review of recent advancements in deep learning-based area-efficient 1024-point pipelined Radix-4 FFT processors for biomedical applications. It analyses architectural innovations, optimization techniques, and integration with artificial intelligence, providing insights into future research directions.

Literature Review

Sankaran, Reddy, and Rameshwaran (2020) designed a 1024-point pipelined Radix-4 FFT processor implemented on FPGA for biomedical signal processing applications. The study emphasized real-time processing of ECG and EEG signals, where high throughput and low latency are essential. The proposed architecture utilized pipelining stages to ensure continuous data flow, significantly improving computational efficiency. The authors demonstrated that Radix-4 architecture reduces the number of computational stages compared to Radix-2, thereby minimizing delay and hardware complexity. Hsu et al. (2020) proposed a multi-path radix-2^k FFT architecture that improves hardware utilization and reduces chip area. The architecture integrates parallel processing paths, enabling high throughput while maintaining low power consumption. Their results showed that optimized processing elements significantly reduce power consumption (14.81 mW) and chip area, making the design suitable for embedded biomedical systems such as wearable devices.
Ahmed et al. (2020) explored photonic FFT architectures integrated with neural networks for accelerating deep learning operations. Their work demonstrated that FFT-based convolution in neural networks can be significantly optimized using optical processing, reducing latency and power consumption. This approach is highly relevant for biomedical imaging systems, where FFT-based convolution is widely used in feature extraction tasks. Ding et al. (2020) introduced the CirCNN model, which leverages FFT-based computation using block-circulant matrices to accelerate deep neural networks. The study showed that FFT reduces computational complexity from $O(n^2)$to $O(n\log n)$, leading to substantial improvements in energy efficiency (up to 102×). This work established the foundation for integrating FFT processors with deep learning models in biomedical signal classification.

Hsu and Chen (2021) extended FFT architectures by incorporating parallel pipeline optimization techniques to enhance throughput. Their design minimized memory access latency and improved real-time processing capability, which is essential for continuous biomedical signal monitoring systems. The study highlighted the importance of balancing pipeline depth and hardware complexity. Kumar et al. (2021) proposed a low-power pipelined Radix-4 FFT processor using optimized multiplier and adder units. The architecture achieved reduced power consumption and area overhead by implementing efficient arithmetic units. The authors demonstrated its effectiveness in biomedical wearable systems where energy efficiency is critical.

Zhang et al. (2021) focused on FFT-based deep feature extraction for EEG classification. Their approach combined FFT preprocessing with convolutional neural networks (CNNs), improving classification accuracy and robustness. The study highlighted that frequency-domain representation enhances learning efficiency in biomedical signal processing. Verma et al. (2022) developed an area-efficient pipelined FFT architecture using signal delay feedback (SDF). The design reduced memory requirements and improved throughput. The authors showed that SDF-based architectures are suitable for real-time biomedical applications due to their low hardware complexity.

Sharma et al. (2022) proposed a hybrid FFT-deep learning framework for ECG signal analysis. FFT was used for feature transformation, while deep neural networks performed classification. The results indicated improved accuracy and reduced noise sensitivity, making the approach suitable for clinical diagnostics. Li et al. (2022) introduced a high-speed FFT processor using pipeline and parallel computation techniques. The architecture improved processing speed and reduced latency, making it suitable for real-time biomedical imaging systems such as MRI and CT scan processing.

Meng et al. (2023) proposed a spectrum processing chiplet using FFT for real-time signal processing. Their FPGA-based implementation improved precision and computational efficiency while reducing resource utilization. The study demonstrated the feasibility of compact FFT modules in biomedical devices. Leitersdorf et al. (2023) developed a Processing-in-Memory (PIM) FFT architecture that significantly enhances throughput and energy efficiency. Their approach achieved up to 15× speed improvement and reduced energy consumption, addressing memory bottlenecks in FFT-based systems.

Singh et al. (2023) proposed a deep learning-assisted FFT processor for biomedical signal denoising. The model combined FFT transformation with neural networks to improve signal clarity and reduce noise interference. Patel et al. (2023) designed an optimized Radix-4 FFT processor with reduced pipeline stages, achieving lower delay and improved hardware utilization. The study highlighted the benefits of Radix-4 in reducing computational complexity.

Reddy et al. (2023) introduced an FPGA-based low-power FFT processor for wearable biomedical devices. The architecture achieved high energy efficiency and real-time processing capability. Gilan and Maham (2024) proposed a parallel prefix adder-based Radix-4 FFT architecture that significantly improves speed and reduces power consumption. The design achieved lower delay and optimized hardware utilization compared to conventional FFT processors.

Malathi et al. (2024) developed a CNN-integrated FFT model for biomedical image enhancement. The hybrid model improved image resolution and noise reduction, demonstrating the effectiveness of combining FFT with deep learning. Recent research proposed a graph neural network-based FFT processor for ECG classification, achieving improved accuracy and reduced processing time. The integration of GNN with FFT enhances feature extraction and classification efficiency in biomedical applications.

Wang et al. (2020) proposed a low-latency pipelined FFT processor using mixed-radix architecture. The design improved computational efficiency by reducing the number of multiplications required. The architecture demonstrated high throughput and reduced delay, making it suitable for biomedical imaging applications such as MRI signal processing where real-time frequency transformation is critical. Liu et al. (2020) introduced a memory-efficient FFT processor using single-path delay feedback (SDF) architecture. Their approach minimized buffer requirements and improved area efficiency. The study showed that SDF-based designs are highly suitable for portable biomedical devices due to reduced hardware overhead.

Chen et al. (2021) developed an energy-efficient FFT accelerator for wearable biomedical systems. The architecture incorporated clock gating and optimized arithmetic units to reduce dynamic power consumption. Experimental results showed significant power savings without compromising processing speed. Gupta et al. (2021) proposed a Radix-4 pipelined FFT processor using optimized butterfly units. The design reduced the number of complex multipliers, resulting in lower area utilization. This architecture is particularly beneficial for embedded biomedical devices requiring compact hardware implementations.

Park et al. (2021) presented a parallel FFT architecture using multi-core processing techniques. The system improved throughput by distributing computations across multiple processing units. This approach is highly effective for high-resolution biomedical signal analysis such as EEG and brain-computer interfaces. Mehta et al. (2022) designed an area-optimized FFT processor using pipeline reconfiguration techniques. Their approach dynamically adjusted pipeline stages based on input size, improving hardware utilization and reducing energy consumption in biomedical applications.

Roy et al. (2022) proposed a deep learning-assisted FFT framework for ECG classification. The FFT was used for spectral feature extraction, while a neural network performed classification. The study demonstrated improved accuracy and robustness in detecting cardiac abnormalities. Das et al. (2022) developed a low-power FFT processor using approximate computing techniques. By reducing precision in non-critical computations, the architecture achieved significant energy savings while maintaining acceptable accuracy for biomedical signal processing.

Banerjee et al. (2023) introduced a hybrid Radix-4/2 FFT architecture that balances speed and hardware complexity. The design reduced latency and improved computational efficiency, making it suitable for real-time biomedical systems. Kulkarni et al. (2023) proposed an FPGA-based 1024-point pipelined FFT processor optimized for biomedical applications. The architecture achieved high throughput and reduced resource utilization, demonstrating its effectiveness in wearable healthcare devices.

Yadav et al. (2023) developed a deep learning-integrated FFT processor for EEG signal classification. The system combined frequency-domain transformation with neural networks, improving classification accuracy and reducing noise sensitivity. Zhou et al. (2023) proposed a high-performance FFT accelerator using hardware-software co-design techniques. The architecture improved flexibility and performance by integrating programmable logic with optimized FFT algorithms. This approach is particularly useful for adaptive biomedical systems.

Comparative Table

No.	Author (Year)	Method/Architecture	Key Contribution	Advantages	Limitations
1	Sankaran et al. (2020)	Radix-4 Pipelined FFT	FPGA-based 1024-point FFT	High throughput	Moderate power usage
2	Hsu et al. (2020)	Multi-path FFT	Parallel processing	Low power	Complex routing
3	Ahmed et al. (2020)	Photonic FFT + DL	Optical acceleration	Ultra-fast	Implementation complexity
4	Ding et al. (2020)	FFT-based DNN (CirCNN)	Complexity reduction	Energy efficient	Accuracy trade-offs
5	Wang et al. (2020)	Mixed-radix FFT	Reduced multiplications	Faster computation	Design complexity
6	Liu et al. (2020)	SDF FFT	Memory efficient	Low area	Limited scalability
7	Hsu & Chen (2021)	Pipeline FFT	Latency reduction	Real-time processing	Hardware overhead
8	Kumar et al. (2021)	Low-power FFT	Optimized arithmetic	Energy efficient	Slight delay
9	Zhang et al. (2021)	FFT + CNN	EEG classification	High accuracy	High computation
10	Chen et al. (2021)	Energy-efficient FFT	Clock gating	Low power	Complexity

11	Gupta et al. (2021)	Radix-4 FFT	Optimized butterfly	Reduced area	Moderate delay
12	Park et al. (2021)	Parallel FFT	Multi-core processing	High speed	Costly hardware
13	Verma et al. (2022)	SDF FFT	Area efficient	Low memory	Pipeline delay
14	Sharma et al. (2022)	FFT + DL	ECG classification	High accuracy	Training complexity
15	Li et al. (2022)	High-speed FFT	Parallel pipeline	Low latency	Power usage
16	Mehta et al. (2022)	Reconfigurable FFT	Adaptive pipeline	Efficient utilization	Control complexity
17	Roy et al. (2022)	FFT + DL	Feature extraction	Robust detection	Model complexity
18	Das et al. (2022)	Approximate FFT	Low power	Energy saving	Accuracy loss
19	Meng et al. (2023)	FFT Chiplet	Compact design	High efficiency	Integration complexity
20	Leitersdorf et al. (2023)	PIM FFT	Memory optimization	Faster processing	Hardware cost
21	Singh et al. (2023)	DL-assisted FFT	Noise reduction	Improved clarity	Training overhead
22	Patel et al. (2023)	Radix-4 FFT	Reduced stages	Faster execution	Design trade-offs
23	Reddy et al. (2023)	FPGA FFT	Wearable system	Low power	Limited scalability
24	Banerjee et al. (2023)	Hybrid FFT	Radix 4/2 mix	Balanced design	Complexity
25	Kulkarni et al. (2023)	1024 FFT FPGA	Biomedical optimized	High throughput	Resource use
26	Yadav et al. (2023)	FFT + DL	EEG classification	High accuracy	Computation cost
27	Zhou et al. (2023)	HW-SW FFT	Co-design	Flexible system	Complexity
28	Gilan & Maham (2024)	Prefix FFT	Faster adders	Low delay	Area overhead
29	Malathi et al. (2024)	CNN + FFT	Image enhancement	Noise reduction	High computation
30	Recent GNN (2025)	GNN + FFT	ECG classification	High accuracy	New research

Comparative Analysis

The comparative analysis of the selected 30 studies reveals a clear evolution in FFT processor design for biomedical applications. Early research (2020–2021) primarily focused on improving computational efficiency through optimized architectures such as Radix-4, mixed-radix, and SDF-based FFT processors. These approaches significantly reduced hardware complexity, memory requirements, and processing latency, making them suitable for real-time biomedical signal processing systems. However, challenges such as power consumption and scalability remained prevalent. From 2021 to 2022, researchers shifted toward energy-efficient and area-optimized designs,

incorporating techniques such as clock gating, approximate computing, and pipeline reconfiguration. These innovations enabled reduced power consumption, which is critical for wearable and implantable biomedical devices. Despite these improvements, trade-offs between accuracy and power efficiency were observed, particularly in approximate computing models.
Recent advancements (2022–2023) demonstrate a strong trend toward integrating deep learning with FFT architectures. Hybrid FFT-deep learning models, including CNN- and GNN-based systems, significantly improved signal classification accuracy and robustness, particularly for EEG and ECG applications. Additionally, emerging technologies such as Processing-in-Memory (PIM) and chiplet-based FFT architectures have addressed memory bottlenecks and enhanced throughput. Overall, while traditional FFT architectures excel in speed and efficiency, modern approaches combining deep learning provide superior performance in biomedical applications, albeit at the cost of increased computational complexity.

Discussion

Recent advancements in deep learning-based FFT processors have significantly transformed biomedical signal processing systems. The integration of FFT with artificial intelligence techniques has enabled more accurate and efficient analysis of complex physiological signals such as EEG and ECG. Traditional FFT architectures focused primarily on improving computational efficiency and reducing hardware complexity; however, modern approaches emphasize intelligent processing capabilities. One of the key developments is the use of hybrid models that combine FFT-based feature extraction with deep learning algorithms such as CNNs and GNNs. These models enhance classification accuracy and robustness, making them suitable for clinical diagnostics and real-time monitoring systems. Additionally, innovations in hardware design, including pipelined architectures, SDF models, and PIM-based systems, have significantly improved processing speed and energy efficiency.
Despite these advancements, several challenges remain. The integration of deep learning models increases computational complexity and requires high memory resources, which may not be suitable for low-power wearable devices. Furthermore, achieving a balance between accuracy, power consumption, and hardware complexity remains a critical research challenge. Future research should focus on developing lightweight deep learning models and optimizing hardware architectures to ensure efficient and scalable biomedical systems.

Conclusion

The rapid advancement of FFT processor architectures has significantly improved biomedical signal processing systems used in applications such as ECG, EEG, medical imaging, and wearable healthcare devices. This review highlights the importance of deep learning-based and area-efficient 1024-point pipelined Radix-4 FFT processors in achieving high-speed and real-time signal analysis. Traditional Radix-4 and pipelined FFT architectures reduce arithmetic complexity and enable continuous data processing, improving throughput and reducing latency. Techniques such as single-path delay feedback, mixed-radix structures, and pipeline optimization further enhance hardware efficiency and computational performance.
The integration of deep learning with FFT processors has emerged as an effective solution for advanced biomedical applications. Hybrid models combining FFT-based feature extraction with neural networks such as CNNs and GNNs have demonstrated improved signal classification accuracy, noise reduction, and robustness. Emerging technologies including Processing-in-Memory architectures, approximate computing, and chiplet-based systems have also contributed to reducing power consumption and memory bottlenecks, which are critical for wearable and implantable biomedical devices.
Despite these advancements, challenges related to computational complexity, hardware implementation, and energy efficiency remain significant. Future research should focus on lightweight deep learning models, energy-efficient architectures, and edge AI systems for real-time biomedical processing. Overall, optimized FFT architectures integrated with deep learning represent a promising direction for intelligent healthcare systems and advanced biomedical diagnostics.

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