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Clock-Gated Dual Edge-Triggered Flip-Flop Architectures for Low-Power VLSI Systems

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Abstract

As digital systems move toward ultra-low power operation and higher performance, reducing clockrelated power has become a major challenge in modern VLSI design, from the clock network alone can consume a large portion of total chip power. This work presents a Dual Edge Triggered flip-flop clock-gated architecture aimed at minimizing dynamic power dissipation while maintaining high-speed performance. Both rising and falling clock edges are captured by Dual Edge Triggered flip-flops, allowing the frequency of clock to be reduced for the same throughput, thereby lowering switching losses; however, conventional DET designs still suffer from unnecessary clock transitions during idle conditions. To overcome this limitation, a fine-grain clock gating mechanism is introduced as the primary contribution of this work, where gating logic intelligently disables clock activity when data transitions are absent, significantly reducing switching power in both the flip-flop and the clock distribution path. Six DET flip-flop architectures—SDET, TSPC-SDET, FS-TSPC-DET, STC-DET, LPLD-DET, and LPHD-DET—are designed and simulated using predictive 45nm CMOS technology, and comprehensive SPICE simulations are performed to evaluate propagation delay, average power, and area across 0.5 V to 1.0 V of voltage supply at 50 MHz. Simulated results show that integrating clock gating achieves substantial power savings compared to non-gated DET designs with minimal delay overhead. Among the evaluated designs, the proposed clock-gated LPHD-DET and LPLD-DET flip-flops provide the best performance balance between speed, area, and power optimization, making the architecture highly applicable for low-power VLSI systems such as IoT devices, wearable electronics, and batteryoperated embedded systems.

Keywords: Double Edge Triggered; Clock Gating; Flip-Flop Design; Low-Power VLSI; 45 nm CMOS Technology; Energy-Efficient Digital Circuits.

How to Cite This Article

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Introduction

In modern digital systems, the demand for high performance and low power consumption has become improve because of the rapid growth of portable and battery-operated devices. A significant portion of power in VLSI circuits is consumed by the clock distribution network, which continuously switches regardless of data activity. This unnecessary switching leads to increased dynamic power dissipation, making power optimization a critical challenge in contemporary chip design.

Flip-flops are basic building blocks of sequential circuits and play a major role inevaluating the overall power consumption and working speed of a system.

Among many designs, Dual Edge Triggered (DET) flip-flops have gained attention because they gain data on both the edges of the clock signal. This ability makes the system to manage the same data throughput at a lower frequency of the clock, thereby reducing switching activity and power consumption. However, conventional DET flip-flops still suffer from inefficiencies due to continuous clock transitions even during idle conditions. To address these challenges, clock gating techniques have been introduced as an effective method for reducing unnecessary clock activity. By disabling the clock signal when no data transition occurs, clock gating significantly minimizes switching power in both the flip-flop and the clock network. In this context, the proposed work focuses on designing a clock-gated DET flip-flop architecture that integrates fine-grain gating mechanisms to enhance power efficiency without compromising performance. The proposed system is implemented using 45nm CMOS technology and evaluated through SPICE simulations to analyse key performance parameters such as power consumption, propagation delay and area. Multiple DET architectures are considered to identify the most efficient design. This approach aims to attain an efficient balance between speed, power, and area, making it suitable for modern applications such as IoT devices, wearable electronics, and low-power embedded systems.

Related Work

CMOS Technology (45nm)

45nm CMOS technology is a popular semiconductor fabrication process that enables high-speed, lowpower, and high-density VLSI circuit design. With a minimum transistor feature size of 45 nanometers, it allows millions of transistors to be integrated into a

compact chip area, improving performance while reducing power consumption and area. The technology provides an effective balance between speed, energy efficiency, and scalability, making it suitable for modern digital systems such as clockgated Dual Edge Triggered (DET) flip-flops. Due to its reliability and optimized transistor sizing, 45nm CMOS technology is extensively used in low-power applications including IoT devices, wearable electronics, embedded systems, and advanced VLSI architectures.

High Transistor Density

One of the most significant features of 45nm technology is its ability to integrate a large number of transistors within a very small chip area. Due to the reduced feature size, more logic elements can be packed into a single integrated circuit, enabling the design of complex systems such as processors and signal processing units. This high density not only improves functionality but also reduces the overall chip size and cost.

Reduced Supply Voltage

45nm CMOS technology operates at lower supply voltages, typically ranging from 0.5V to 1.0V. Lowering the supply voltage directly reduces dynamic intake of power, as power consumption is proportional to the square of the supply voltage. This system is important for low power portable devices such as IoT systems and wearable electronics, where energy efficiency is critical.

Lower Capacitance

As transistor dimensions shrink, parasitic capacitances associated with the device also decrease. Lower capacitance reduces charge and discharge time in a circuit, thereby decreasing delay and dynamic power consumption. This contributes to improved overall circuit efficiency and performance.

Support for Advanced Power Reduction Techniques

45nm CMOS technology supports modern power optimization techniques such as clock gating, power gating, and dynamic voltage scaling. These techniques help in reducing unnecessary switching activity and leakage power, making the circuits more energy-efficient. This feature is particularly beneficial in designs like DET flip-flops where clock power plays a major role.

Improved Performance-to-Power Ratio

This technology node offers a better balance between performance and power consumption compared to older technologies like 90nm or 65nm. Designers can achieve higher speed without significantly increasing power consumption.

Role In the Proposed System

- Used as the base technology for designing and simulating DET flip-flop architectures.
- Enables accurate evaluation of power, delay, and area parameters using SPICE tools.
- Supports low-voltage operation, which is critical for reducing power consumption.
- Facilitates implementation of fine-grain clock gating techniques.
- Helps in achieving an optimal performance balance between speed, power, and area.
- Makes the system suitable for real-world applications like IoT and embedded systems.

Power Gating in CMOS Circuits

As CMOS technology scales into nanometer regions, In VLSI design leakage of power has become a major concern. Both static and dynamic power dissipation increase significantly due to reduced transistor dimensions. To address this issue, power gating is widely used as an optimized technique is used in idle conditions to reduce leakage power. In this method, a sleep transistor is inserted between the supply (VDD) or ground (VSS) and the logic circuit, which disconnects the circuit from the power source when not in use. This helps in cutting off the leakage current path, thereby significantly reducing static power consumption with minimal impact on performance. Power gating, commonly referred to as Multi-Threshold CMOS (MTCMOS), makes use of high-threshold voltage transistors that function as sleep transistors to minimize leakage power consumption.

Working of Power Gating

Power gating works by introducing sleep transistors (PMOS header or NMOS footer) that control the connection between the circuit and power rails. During active mode, the sleep transistor is ON, allowing normal circuit operation. In sleep mode, the transistor is turned OFF, isolating the circuit and reducing leakage current. The concept of virtual VDD and virtual VSS is used, where the internal circuit is disconnected from actual supply lines. However, turning OFF the circuit gradually discharges internal nodes, which may increase short-circuit current during transitions.

Types of Power Gating

Power gating can be integrated in two major ways:

1. Fine-Grain Power Gating (FGPG): Fine-grain power gating applies sleep transistors at the individual cell level. This allows precise control over leakage reduction but increases area overhead and introduces timing challenges due to voltage variations between cells. It is useful when selective power saving is required, and it can reduce leakage power significantly (up to 10×). However, careful design is needed to avoid performance degradation.

2. Coarse-Grain Power Gating (CGPG): Coarse-grain power gating applies sleep transistors at block or module level instead of individual cells. It uses shared virtual power networks and provides better area efficiency with reduced sensitivity to process variations. CGPG can be implemented using ring-based or column-based structures, making it more practical for large circuits. It offers a good balance between power saving and design complexity.

Important Parameters in Power Gating

Several parameters must be carefully selected for effective power gating:

- Power Gate Size: Determines the ability to handle switching current; larger size reduces voltage drop.
- Slew Rate: Controls switching speed of sleep transistor; affects performance and delay.
- Switching Capacitance: Limits how many circuits can be turned ON/OFF simultaneously.
- Rush Current: Sudden current flow during switching can disturb power integrity.
- Leakage Optimization: Proper transistor selection helps minimize leakage current.

Advanced Power Gating Techniques

- Sleep Technique: Uses sleep transistors to disconnect power supply during idle mode, reducing leakage.
- Zigzag Technique: Places sleep transistors in a pattern to reduce wake-up delay and improve efficiency.
- Stack Technique: Splits a transistor into two smaller transistors to reduce leakage but increases delay.
- Sleepy Stack Technique: Combines sleep and stack techniques to achieve better leakage reduction while maintaining state retention.
- Dual Sleep Technique: Uses additional PMOS and NMOS transistors to control leakage more effectively in sleep mode.
- Dual Stack Technique: Uses stacked transistors in both pull-up and pull-down networks to reduce leakage through increased threshold voltage and reduced DIBL effect.

Experiments

Single Edge Triggered Flip-Flop

The Master Slave Flip-Flop (MSFF) comprises of two latch structures, one a master-latch and other a slave-latch. Master slave is an improvement to the latch design called an edge-triggered flip-flop which permits state changes to occur briefly as the clock pulse shifts from 0 to 1 or 1 to 0. It is dubbed an edge triggered flip-flop because it is claimed to trigger on the edges of the clock pulse. A rising edge or positive edge trigger means a flip-flop is functioning at a transition in clock signal from low to high whereas a falling edge or negative edge trigger can cause the flipflop to function at a transition in clock signal from high to low. A flip-flop which is work either in rising or falling edge of a clock signal is referred as Single Edge Triggered Flip-Flops (SETFFs). In other words, the outcome changes its state only at a transition in clock from 0-1 or from 1-0 but not both.

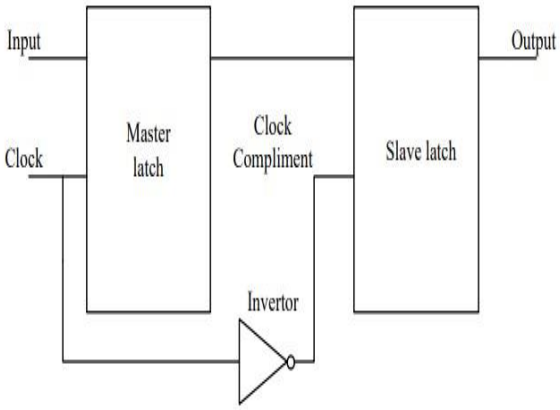

Fig. 1. *Block diagram of master-slave flip-flop*

Dual Edge Triggered Flip-Flop

By comparing with single edge triggered flip-flops, Dual Edge Triggered Flip-Flops (DETFFs) helps in lower the clock frequencies to one-half while maintaining the same data throughput, even if the clock frequency is ordered by circuit requirements. It is a digital data storage element which pick data in both the edges of the clock signal (rising and falling edges). In contrast to single edge triggered flip-flop capture date only on one edge of the clock signal (either in rising or falling edge of the signal). DETFF transfer date two times during a single clock cycle. This make the system reduce the required clock frequency while it maintain same data throughput. DETFF is one of the best way to reduce power consumption in digital ciruits with fewer inter switching activities and fewer clock-controlled components. More energy get wasted when internal nodes switch frequently that means circuit with lower switching will consume less energy, also we can say that static circuit usually consume less power than dynamic circuit because dynamic circuits require continuous precharge and discharge operations during every clock cycle, which increases power dissipation. Normally, conventional flip-flops capture data only on one clock edge (rising or falling edge). However, DETFFs capture data on both edges of the clock signal. Because of this, the same amount of data can be transferred even if the clock frequency is reduced by 50%. Reducing the clock frequency lowers the switching activity in the clock network, which significantly decreases overall power consumption.

Pulse Triggered Flip-Flop

Pulse Triggered Flip-Flops (P-FFs) are widely used in high-speed and low-power digital systems as another way of using Master-Slave Flip-Flops (MSFFs). Unlike MSFFs that require two latches, PFFs use only a single latch along with a pulse generator, reducing circuit complexity, area, and power consumption while improving speed. They operate similarly to master-slave flip-flops when the clock pulse width is sufficiently narrow and are less sensitive to clock skew. P-FFs also support time borrowing with negative setup time, enhancing performance. Based on pulse generation methods, PFFs are classified into explicit and implicit types. Explicit P-FFs use delay-chain based pulse generators, which increase clock power consumption, while implicit P-FFs generate pulses through controlled discharge paths but may suffer from longer discharge delays that can affect performance.

Sense Amplifier Based Flip-Flop

This type operates in pipeline structures which usually are synchronous. At lower voltage levels it has been observed that the circuit suffers from speed degradation. The strength of the driving transistor due to the process variation changes drastically as the supply voltage decreases, which in turn may degrade the functionality of the flip-flop resulting in inappropriate power consumption. To improve the performance of the flip-flops, intensive researches are been carried out. It mainly contains two parts, one is differential stage and another is slave latching stage. Differential sensing stage is used for detect or sense the input data very fast; it captures the input data at the positive edge of the clock

signal. After the sensing stage captures the data, the slave latch stores and holds the output value stable, this was done by slave latching stage. When one data is captured that should be stay or output remains unchanged and stable until the next positive half cycle.

Self-Gated Flip-Flop

In synchronous digital systems, all flip-flops ideally receive the clock signal concurrently. However, it effects parasitic, interconnect delays, voltage variations, temperature changes, and other non-ideal factors cause clock skew and jitter, leading to timing inaccuracies. Since clock distribution networks consume a major portion of total system power, especially in low-power and high-speed VLSI circuits, minimizing clock power consumption and maintaining signal integrity are critical challenges.

Clock skew refers to the difference between the expected and actual arrival times of clock edges, and excessive skew can severely affect system performance and reliability. Most designs can tolerate only a small amount of skew, typically less than 10% of the clock period. Therefore, efficient clock synchronization and low-power clock distribution techniques are essential for modern high-performance digital systems.

Existing System

Earlier research on Dual Edge Triggered (DET) flip-flops mainly focused on 65 nm CMOS technology to improve data throughput by capturing data on both clock edges. Several architectures such as SDET, TSPC-SDET, FS-TSPC-DET, STC-DET, LPLDDET, and LPHD-DET were developed, but most works emphasized basic circuit design and functional simulation with limited optimization techniques. The performance evaluation was generally restricted to conventional methods, with less focus on advanced power reduction, propagation delay optimization, and area efficiency. Comparative analysis among multiple DET architectures was also limited, making it difficult to identify the most efficient design.

Additionally, earlier systems did not adequately address technology scaling issues such as leakage current, variability, and dynamic power reduction when moving to smaller nodes like 45 nm CMOS. Clock gating techniques for minimizing clock power consumption were also not widely implemented. As a result, existing DET flip-flop designs were less work for modern low-power consumption applications such as IoT devices, wearable electronics, and batteryoperated systems, where high energy efficiency and scalability are essential.

Proposed System

The proposed system introduces a clockgated Dual Edge Triggered (DET) flip-flop architecture designed to achieve low power usage and high-speed performance in modern VLSI systems. Unlike conventional flip-flops, the proposed design focuses on minimizing unnecessary clock activity, which is one of the major contributors to dynamic power dissipation. By integrating advanced clock gating techniques with DET operation, the system significantly improves energy efficiency while maintaining high data throughput. In this approach, DET flip-flops capture data on both the rising and falling edges of the clock signal**,** this will reduce clock frequency while maintain same throughput singleedge designs.

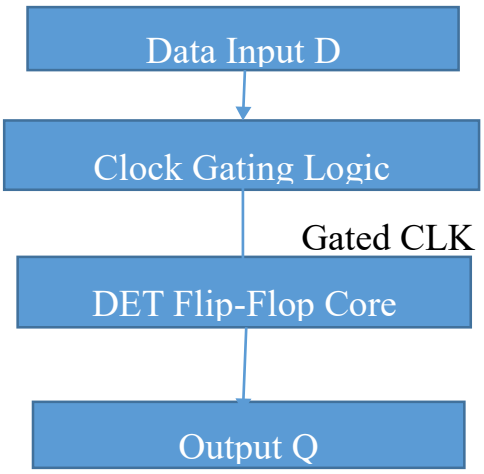

Fig. 2. *Block Diagram*

As a result, switching activity in the clock network is reduced, leading to lower dynamic power consumption without compromising performance. A key contribution of the proposed system is the implementation of a fine-grain clock gating mechanism**.** This mechanism intelligently monitors data transitions and disables the clock signal when no change in input data is detected. By preventing unnecessary clock toggling in idle conditions, the design effectively reduces switching power in both the flip-flop and the clock distribution network.

The system includes the design and analysis of six different DET flip-flop architectures, namely SDET, TSPC-SDET, FS-TSPC-DET, STC-DET, LPLD-DET, and LPHD-DET. Each architecture is implemented and evaluated to study its performance characteristics under the same operating conditions. This comprehensive comparison helps in identifying the most efficient design in terms of power, delay, and area.

The proposed designs are implemented using predictive 45nm CMOS technology, which provides improved scalability, reduced capacitance, and better performance compared to older technology nodes. Simulations are carried out using SPICE tools across a range of supply voltages from 0.5 V to 1.0 V at an operating frequency of 50 MHz. Key performance parameters such as propagation delay, average power consumption, and area used are analysed to ensure optimal design efficiency. Simulation results demonstrate that the integration of clock gating leads to significant power reduction compared to non-gated DET flip-flops, with only a minimal increase in delay. Among all the evaluated architectures, the clock-gated LPHD-DET and LPLD-DET flip-flops show the best trade-off between power, speed, and area.

Methodology

Data Input (D)

The Data Input (D) acts as the primary source of information for the flip-flop circuit, providing the binary signal that needs to be stored and processed. It continuously supplies either a logic 'low' or logic 'high' to the system, ensuring that the circuit always has valid input data available for operation. This input signal is directly connected to the internal nodes of the flip-flop and is also monitored by the clock gating logic to determine whether a transition has occurred.

The value present at the data input plays a major role in deciding the next state of the output, as it represents the data that will be captured during the triggering event of the clock. Since the input can change at any time due to external conditions or preceding circuit stages, the flip-flop must be designed to handle asynchronous variations in the input signal without causing instability. Before the clock edge occurs, the input data is prepared and stabilized, ensuring that it is correctly captured when the clock triggers the flip-flop. The clock gating logic observes changes in the input signal and allows clock propagation only when a transition is detected, preventing unnecessary switching activity. This coordination between the data input and clock signal ensures efficient operation and reduced power consumption. Overall, the Data Input (D) serves as a continuously active signal that determines the behaviour of the flip-flop, enabling accurate data storage during clock events while supporting lowpower operation through controlled clock activity.

Clock Gating Logic

The clock gating logic is a key power-saving block in the circuit, and its main role is to control when the flip-flop should actually receive the clock signal. Instead of allowing the clock to continuously toggle (which wastes power), it intelligently decides whether the clock should be passed or blocked based on the input condition. When the clock signal and a control signal enter this block, the clock gating logic first evaluates whether the flip-flop needs to perform any operation.

This decision is based on the input condition or enable signal coming from the system. If the data stored in the flip-flop does not need to change, there is no need to activate the clock, and this helps in reducing unnecessary switching activity. If the condition indicates that a data update is required, the logic enables the clock signal. In this case, the original clock is allowed to pass through the gating circuit, meaning the flip-flop will become active and ready to capture new data. However, if the condition is not satisfied, the clock signal is blocked or disabled, preventing the flipflop from toggling. In digital circuit, clock switching is one of the major sources of dynamic power consumption.

After this decision-making process, the block generates a gated clock signal, which is essentially a controlled version of the original clock. This gated clock only exists when the system truly requires data processing. Otherwise, it remains inactive, saving energy. Finally, this gated clock signal is forwarded to the DET (Double Edge Triggered) flip-flop core, where it is used for controlled data capturing. Because of this gating mechanism, the flip-flop operates only when necessary, leading to improved power efficiency, reduced switching activity, and overall better performance of the digital system.

DET Flip-Flop Core

The DET (Double Edge Triggered) flip-flop core is a high-performance sequential circuit that improves data throughput and reduces power consumption by capturing data on both the rising and falling edges of the clock signal. Unlike conventional single-edge flip-flops, it processes data twice in one clock cycle without increasing clock frequency, making it suitable for high-speed and low-power applications. The circuit uses internal latches that respond to opposite clock edges, ensuring proper synchronization and stable data storage. The output remains steady between valid clock transitions, reducing unnecessary switching activity and improving energy efficiency.

When combined with clock gating logic, the DET flipflop minimizes unwanted clock transitions, significantly lowering dynamic power consumption. Careful timing design also prevents setup, hold time, and metastability issues, ensuring reliable operation in synchronous systems. Overall, the DET flip-flop core enhances speed, power efficiency, and system performance, making it suitable for modern VLSI systems, processors, IoT devices, and advanced lowpower digital architectures.

Output (Q)

The output (Q) of the DET flip-flop core is the final storage node that provides the synchronized and processed data to the digital system. The output updates only at valid clock transitions, where the flipflop captures input data on both rising and falling edges of the clock signal. Between these transitions, the output remains stable, ensuring reliable and glitchfree operation for downstream circuits.

By updating data twice within a single clock cycle, the DET flip-flop improves data throughput while maintaining proper timing synchronization. The stable output is then forwarded to combinational logic blocks, registers, or other sequential circuits for further processing. Overall, the Q output ensures accurate data propagation, stable system performance, low power consumption, and efficient operation in high-speed VLSI and clock-gated digital systems.

Advantages

- The proposed clock-gated Dual Edge Triggered (DET) flip-flop significantly reduces dynamic power consumption by minimizing unnecessary clock switching through fine-grain clock gating.
- High-speed performance is achieved using DET flip-flops that capture data on both rising and falling clock edges, improving overall efficiency.
- The architecture is optimized for 45 nm CMOS technology and evaluated across six DET designs to identify the best trade-off between power, delay, and area.
- The proposed low-power and energy-efficient design is well suited for contemporary VLSI applications, including IoT devices, wearable technologies, and battery-operated embedded systems.

Result

SDET

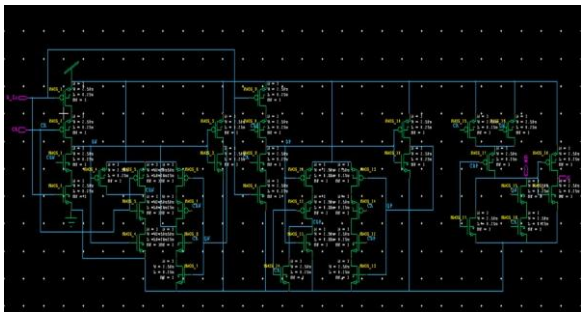

Fig. 3. *Circuit diagram of SDET*

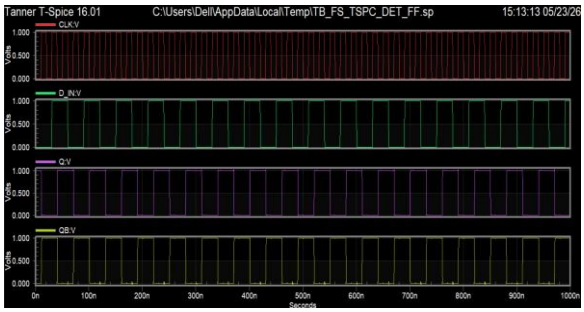

Fig. 4. *Waveform of SDET*

TSPC-SDET

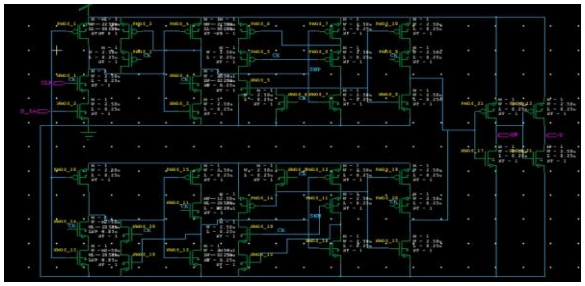

Fig. 5. *Circuit diagram of TSPC-SDET*

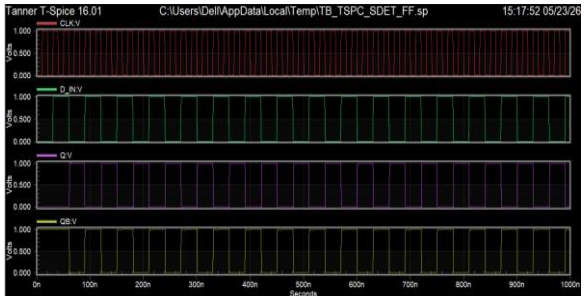

Fig. 6. *Waveform of TSPC-SDET 9.3. LPLD-DET*

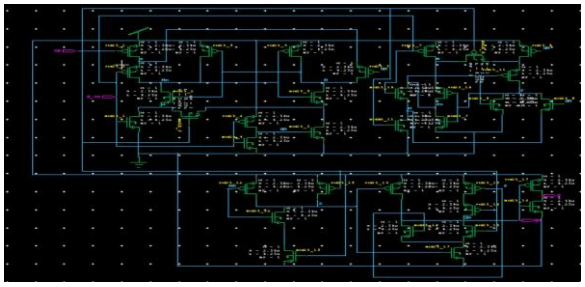

Fig. 7. *Circuit diagram of LPLD-DET*

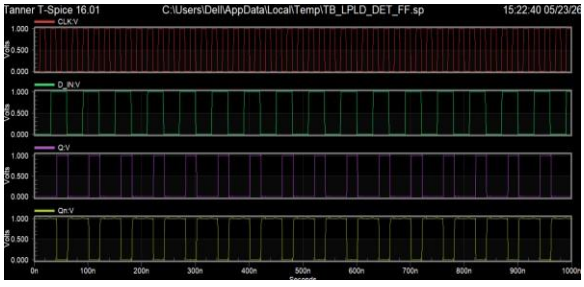

Fig. 8. *Waveform of LPLD-DET*

Conclusion

The proposed clock-gated Dual Edge Triggered (DET) flip-flop architecture effectively achieves low energy usage and high-speed performance. By capturing data on both rising and falling clock edges, it reduces the effective clock frequency while still maintaining the required system throughput. The integration of finegrain clock gating further minimizes unnecessary switching activity, leading to significant power savings in the circuit. Multiple DET flip-flop architectures were designed and analyzed under different operating conditions using 45nm CMOS technology. Simulation results show improvements in propagation delay, power efficiency, and area utilization. Among the evaluated designs, LPHD-DET and LPLD-DET flip-flops provide the best balance between power, speed, and area, making them most suitable for practical low-power VLSI applications.

Future Work

The proposed system can be further enhanced by implementing the design in advanced technology nodes such as 28nm or 7nm, which will help in further reducing power consumption and improving overall performance. The flip-flop architectures can also be integrated into larger digital systems like processors, ALUs, and memory units for real-time validation and practical application analysis. In addition, advanced clock gating techniques such as adaptive or dynamic clock control can be explored to achieve even higher power efficiency. The design can also be optimized for ultra-low voltage operation to support energyconstrained applications like IoT devices and wearable electronics. Finally, hardware implementation using FPGA or ASIC platforms can be carried out to verify real-time performance and practical feasibility of the proposed architecture.

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