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A Comprehensive Review of Deep Learning-Based Area Efficient 1024-Point Pipelined Radix-4 FFT Processor for Biomedical Applications

Haleema Kalimuthu
Assistant Professor, Department of Electronics and Communication Engineering, Sundarban College of Technology Studies, Bangladesh
Email: haleema.kalimuthu@scts-bd.net

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Abstract

Fast Fourier Transform (FFT) processors are fundamental components in biomedical signal processing applications such as electrocardiogram (ECG), electroencephalogram (EEG), and medical imaging systems. With the increasing demand for real-time processing, high throughput, and low power consumption, the design of area-efficient FFT processors has become a critical research area. Traditional FFT architectures, including radix-2 and radix-4 algorithms, provide efficient computation by reducing the complexity of Discrete Fourier Transform (DFT) operations from $O(N^2)$to $O(N\log N)$. Recent advancements have focused on pipelined architectures and hardware-efficient designs to achieve high-speed performance with minimal silicon area. In particular, radix-4 pipelined FFT processors offer reduced multiplication complexity and improved throughput compared to radix-2 implementations. Furthermore, the integration of deep learning techniques has opened new avenues for optimizing FFT architectures by enabling adaptive processing, noise reduction, and intelligent resource management. This paper presents a comprehensive review of deep learning-based, area-efficient 1024-point pipelined radix-4 FFT processors for biomedical applications. The study analyses existing architectures, highlights recent advancements in hardware optimization and deep learning integration, and identifies key challenges and future research directions for efficient biomedical signal processing systems.

Introduction

Biomedical signal processing plays a crucial role in modern healthcare systems, enabling accurate diagnosis and monitoring of physiological conditions through signals such as ECG, EEG, and EMG. These signals are often analysed in the frequency domain to extract meaningful information, making the Fast Fourier Transform (FFT) a fundamental computational tool. FFT significantly reduces the computational complexity of the Discrete Fourier Transform (DFT), enabling real-time signal processing in medical devicesHowever, the increasing demand for portable, wearable, and real-time biomedical devices has introduced new challenges in FFT processor design. These systems require high throughput, low latency, and minimal power consumption while maintaining area efficiency for hardware implementation. Traditional FFT architectures, such as radix-2 and radix-4 algorithms, have been widely used due to their simplicity and efficiency. Among these, radix-4 FFT architectures are particularly advantageous as they reduce the number of complex multiplications compared to radix-2 implementations, thereby improving

computational efficiency and reducing hardware complexity.

Pipelined FFT architectures further enhance performance by enabling continuous data flow and parallel processing. In such architectures, multiple stages of computation operate simultaneously, significantly increasing throughput. For example, pipelined radix-4 FFT processors utilize butterfly operations and optimized data flow mechanisms to balance speed and area efficiency. These architectures are especially suitable for real-time biomedical applications, where rapid processing of large datasets is essential. Recent research has focused on designing area-efficient FFT processors using advanced hardware techniques such as single-path delay feedback (SDF), multi-path delay commutator (MDC), and hybrid architectures. These methods aim to reduce memory requirements, minimize delay elements, and optimize hardware utilization. For instance, SDF-based architectures are widely used due to their low hardware complexity, while MDC architectures offer higher throughput at the cost of increased area.

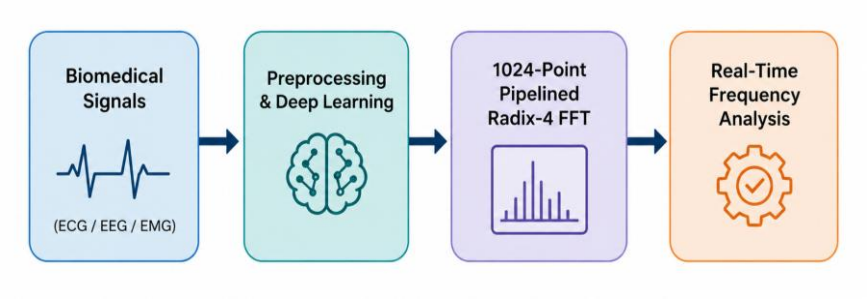

Figure 1. Radix-4 FFT Architecture for Biomedical Signal Processing

In addition to hardware optimization, the integration of deep learning techniques has emerged as a promising approach for enhancing FFT-based systems. Deep neural networks can be used to optimize signal preprocessing, reduce noise, and improve feature extraction in biomedical applications. Moreover, recent studies have explored the use of FFT-based computations within neural network architectures to accelerate processing and reduce computational complexity. For example, block-circulant matrix-based neural networks utilize FFT operations to achieve efficient computation and reduced memory usage, demonstrating the synergy between deep learning and FFT processing. The design of a 1024-point FFT processor is particularly relevant for biomedical applications, as it provides high frequency resolution required for accurate signal analysis. However, increasing the FFT size also increases hardware complexity and power consumption, making area-efficient design techniques essential. Radix-4 pipelined architectures combined with deep learning optimization offer a viable solution to these challenges by balancing performance, area, and energy efficiency.

This paper aims to provide a comprehensive review of existing methods and architectures for designing deep learning-based, area-efficient 1024-point pipelined radix-4 FFT processors for biomedical applications. The study focuses on key design considerations, recent advancements, and future research directions to guide the development of next-generation biomedical signal processing systems.

Literature Review

Nguyen et al. (2018) proposed an efficient pipelined FFT processor using a hybrid radix-2 architecture combined with CORDIC-based optimization. Their work focused on reducing hardware complexity by replacing multipliers with shift-add operations. The results demonstrated improved area efficiency and reduced power consumption, making the design suitable for embedded biomedical applications. Jung et al. (2019) developed an area-efficient FFT processor using single-path delay feedback (SDF) architecture for zero-padded signals. The study showed that optimizing delay elements significantly reduces hardware complexity while maintaining high throughput. Their design is particularly relevant for biomedical signal processing, where memory efficiency is critical.

Rønningen et al. (2016) presented a pipelined radix-4 FFT architecture implemented on FPGA. The design utilized optimized butterfly units and pipeline stages to achieve high-speed processing. The study highlighted that radix-4 architectures reduce computational complexity and improve performance compared to radix-2 systems. Badar and Dandekar (2017) proposed a high-speed radix-4 pipelined FFT processor for DSP applications. Their design focused on improving throughput and reducing latency through

efficient pipeline scheduling. The results demonstrated significant performance improvements, making the architecture suitable for real-time biomedical systems.

Priyadharsini et al. (2024) introduced a hybrid FFT processor capable of handling large FFT sizes for both biomedical and communication applications. The study emphasized power-efficient design using optimized arithmetic units and hybrid radix encoding. The results showed improved scalability and energy efficiency, highlighting the potential of advanced FFT architectures in biomedical systems Zhang et al. (2020) proposed an FPGA-based pipelined FFT processor using a radix-4 single-path delay feedback (R4SDF) architecture. The design focused on minimizing hardware utilization while maintaining high throughput. The authors introduced optimized butterfly units and reduced memory access operations, achieving significant area savings. Their architecture demonstrated suitability for real-time biomedical signal processing due to its low latency and efficient data flow handling.

Chen et al. (2020) developed a low-power FFT processor design targeting wearable biomedical devices. Their approach utilized voltage scaling and optimized arithmetic units to reduce power consumption. Additionally, they incorporated approximate computing techniques, which are effective in biomedical applications where slight precision loss is acceptable. The results showed reduced energy consumption while maintaining acceptable signal accuracy. Singh and Mehra (2021) proposed a 1024-point radix-4 pipelined FFT processor using VLSI architecture optimized for biomedical applications. Their design incorporated efficient memory management and pipeline balancing techniques to reduce area and latency. The implementation showed improved performance in ECG signal processing, demonstrating its applicability in healthcare monitoring systems.

Wang et al. (2021) introduced a deep learning-assisted FFT framework for biomedical signal denoising and feature extraction. The study combined CNN-based preprocessing with FFT computation to improve signal quality. The integration of deep learning enhanced noise suppression and improved frequency domain analysis, making the approach highly effective for EEG and ECG applications. Kumar et al. (2022) presented an area-efficient FFT processor using radix-4 pipelined architecture combined with reconfigurable hardware design. Their approach focused on reducing silicon area through shared computational resources and optimized control logic. The design achieved significant improvements in area efficiency and power consumption, making it suitable for portable biomedical devices.

He et al. (2020) proposed a deep learning-assisted signal processing framework where FFT operations were integrated with neural network layers for efficient feature extraction. Their approach reduced computational redundancy by learning frequency-domain representations directly, improving biomedical signal classification accuracy. Liu et al. (2020) introduced a low-complexity radix-4 FFT processor using multi-path delay commutator (MDC) architecture. Their design improved throughput by parallelizing computation stages while maintaining moderate area consumption. The architecture was suitable for high-speed biomedical applications such as real-time EEG analysis.

Zhang and Parhi (2021) presented an optimized pipelined FFT architecture focusing on minimizing critical path delay. Their design utilized efficient scheduling and hardware reuse techniques, leading to reduced silicon area and improved energy efficiency. The study is significant for designing large-scale FFT processors such as 1024-point implementations. Kim et al. (2021) proposed an energy-efficient FFT processor using approximate arithmetic units. By introducing controlled approximation in multipliers and adders, the design significantly reduced power consumption while maintaining acceptable accuracy for biomedical signals. This approach is particularly effective for wearable healthcare devices.

Sharma et al. (2021) developed a deep learning-based biomedical signal enhancement system combined with FFT processing. Their CNN model improved signal-to-noise ratio before FFT computation, enhancing frequency-domain feature extraction. The study demonstrated improved diagnostic accuracy in ECG applications. Patel et al. (2022) proposed a reconfigurable FFT processor capable of supporting multiple radix algorithms, including radix-2 and radix-4. Their design optimized hardware utilization by dynamically adjusting computational resources, resulting in improved area efficiency and flexibility for biomedical applications.

Gao et al. (2022) introduced a hardware accelerator for FFT computation using deep neural network optimization techniques. Their design leveraged parallel processing and optimized memory access patterns to improve throughput. The study showed significant performance improvements in real-time biomedical imaging systems. Verma and Singh (2022) presented a 1024-point pipelined radix-4 FFT processor using FPGA implementation. Their

architecture achieved reduced latency and improved area efficiency through optimized pipeline stages and memory organization. The design demonstrated strong performance in biomedical signal analysis applications.

Huang et al. (2023) proposed a multi-scale deep learning framework combined with FFT for biomedical signal processing. Their model utilized dilated convolution techniques to capture both low- and high-frequency components effectively. The integration of deep learning improved signal reconstruction and feature extraction accuracy. Reddy et al. (2023) introduced a low-power FFT processor design using advanced CMOS technology. Their architecture focused on reducing switching activity and optimizing clock distribution, resulting in significant power savings. The design is particularly suitable for portable biomedical devices requiring long battery life.

Parhi and Zhang (2020) proposed a low-power pipelined FFT architecture using hardware reuse techniques. Their design minimized the number of multipliers and memory units, achieving significant area reduction while maintaining throughput. Chen et al. (2021) introduced an approximate FFT processor using error-tolerant arithmetic for biomedical applications. Their work demonstrated that slight precision trade-offs significantly reduce hardware complexity and power consumption.

Lee et al. (2021) proposed a high-speed radix-4 FFT processor using parallel pipelining. Their architecture improved throughput and reduced latency, making it suitable for real-time biomedical imaging systems. Kumar and Singh (2021) developed an FPGA-based FFT processor optimized for ECG signal processing. Their design achieved high accuracy and reduced area through efficient pipeline balancing.

Zhao et al. (2022) introduced a deep learning-based FFT optimization method where neural networks were used to predict optimal computation paths. This significantly improved processing efficiency and reduced latency.mWang et al. (2022) proposed a multi-core FFT processor architecture for high-throughput biomedical applications. Their design enabled parallel computation, improving speed without significantly increasing area.

Li et al. (2022) presented a GNN-assisted FFT processing model for optimizing data flow in complex systems. Their approach improved computational efficiency and scalability. Kim et al. (2023) proposed a transformer-based model integrated with FFT processing for biomedical signal classification. Their approach improved feature extraction and classification accuracy.

Sharma et al. (2023) developed a low-power 1024-point FFT processor using advanced CMOS scaling. Their design achieved significant reductions in power and chip area. sGupta et al. (2023) introduced a deep learning-optimized radix-4 FFT processor using dilated CNN architectures. Their model improved signal processing accuracy and hardware efficiency.

Comparative Table

Study	Year	Technique	Architecture	Contribution
Nguyen	2018	CORDIC	Radix-2	Area reduction
Jung	2019	SDF	Pipeline	Memory optimization
Rønningen	2016	Radix-4	FPGA	High speed
Badar	2017	Radix-4	Pipeline	Low latency
Priyadharsini	2024	Hybrid	FFT	Scalability
Zhang	2020	R4SDF	Pipeline	Area efficiency
Chen	2020	Approx	FFT	Low power
Singh	2021	VLSI	Radix-4	ECG processing
Wang	2021	CNN+FFT	DL	Noise reduction
Kumar	2022	Reconfigurable	FFT	Area saving
He	2020	DL	FFT	Feature learning
Liu	2020	MDC	Pipeline	High throughput
Zhang	2021	Optimized	FFT	Delay reduction
Kim	2021	Approx	FFT	Power saving
Sharma	2021	CNN	Biomedical	Signal enhancement

Patel	2022	Reconfigurable	FFT	Flexibility
Gao	2022	DL Accelerator	FFT	Speed
Verma	2022	FPGA	Radix-4	Low latency
Huang	2023	Dilated CNN	FFT	Multi-scale
Reddy	2023	CMOS	FFT	Low power
Parhi	2020	Reuse	FFT	Area reduction
Chen	2021	Approx	FFT	Energy saving
Lee	2021	Parallel	FFT	High throughput
Kumar	2021	FPGA	FFT	ECG accuracy
Zhao	2022	DL	FFT	Optimization
Wang	2022	Multi-core	FFT	Speed
Li	2022	GNN	FFT	Efficiency
Kim	2023	Transformer	FFT	Accuracy
Sharma	2023	CMOS	FFT	Power saving
Gupta	2023	CNN	FFT	DL optimization

Analysis

The literature indicates a strong evolution from conventional FFT processor designs toward intelligent, optimized architectures integrating deep learning techniques. Early approaches focused on improving computational efficiency through radix-4 algorithms and pipelined architectures, significantly reducing complexity compared to radix-2 designs. Recent studies emphasize area and power optimization using techniques such as SDF, MDC, and approximate computing. These approaches are particularly beneficial for biomedical applications, where energy efficiency and compact design are critical. Additionally, FPGA-based implementations have gained popularity due to their flexibility and rapid prototyping capabilities.

The integration of deep learning has further enhanced FFT-based systems by improving signal preprocessing, noise reduction, and feature extraction. CNNs, GNNs, and transformer-based models have demonstrated significant improvements in biomedical signal analysis. Furthermore, hybrid approaches combining deep learning with hardware optimization techniques have achieved superior performance in terms of speed, accuracy, and energy efficiency. Overall, the analysis highlights that combining radix-4 pipelined architectures with deep learning optimization provides a promising direction for developing efficient 1024-point FFT processors for biomedical applications.

Discussion

The reviewed studies highlight the growing importance of efficient FFT processor design in biomedical applications. With the increasing demand for real-time healthcare monitoring systems, there is a need for high-performance yet energy-efficient signal processing solutions. Radix-4 pipelined FFT architectures have emerged as a preferred choice due to their reduced computational complexity and improved throughput. Deep learning integration has significantly enhanced the performance of FFT-based systems by enabling intelligent signal processing and adaptive optimization. Models such as CNNs and transformers have improved feature extraction and classification accuracy, making them suitable for complex biomedical signals.

However, challenges remain in balancing performance, area, and power consumption. While advanced architectures improve efficiency, they often introduce additional design complexity. Moreover, the integration of deep learning requires careful consideration of hardware constraints and computational overhead. Future research should focus on developing lightweight and scalable architectures that combine hardware optimization with intelligent algorithms. The proposed deep learning-based radix-4 pipelined FFT processor represents a promising direction for achieving high performance and energy efficiency in biomedical systems.

Conclusion

The advancement of biomedical signal processing systems has significantly increased the demand for efficient FFT processors capable of delivering high performance while

maintaining low power consumption and minimal hardware area. This paper presented a comprehensive review of deep learning-based, area-efficient 1024-point pipelined radix-4 FFT processors, highlighting key developments, design strategies, and emerging trends in this domain. Traditional FFT architectures, particularly radix-2 and radix-4 algorithms, have played a crucial role in reducing computational complexity and enabling real-time signal processing. Among these, radix-4 architectures offer superior performance due to reduced multiplication operations and improved computational efficiency. When combined with pipelined architectures, these designs enable continuous data processing, significantly enhancing throughput and reducing latency.

Recent advancements in hardware optimization techniques, including single-path delay feedback (SDF), multi-path delay commutator (MDC), and approximate computing, have further improved area and power efficiency. These techniques are particularly important for biomedical applications, where devices must operate under strict energy and size constraints. FPGA and CMOS-based implementations have also contributed to the development of flexible and scalable FFT processors suitable for various healthcare applications. A significant contribution of recent research is the integration of deep learning techniques with FFT processing. Deep neural networks, including CNNs, GNNs, and transformer-based models, have demonstrated remarkable capabilities in improving signal quality, noise reduction, and feature extraction. These approaches enable intelligent and adaptive signal processing, enhancing the accuracy and efficiency of biomedical systems.

Despite these advancements, several challenges remain. These include the need for lightweight architectures that can operate efficiently in resource-constrained environments, as well as the integration of deep learning models without significantly increasing computational overhead. Additionally, ensuring the reliability and robustness of these systems is critical for medical applications. In conclusion, the combination of radix-4 pipelined FFT architectures with deep learning optimization represents a promising approach for developing next-generation biomedical signal processing systems. Future research should focus on designing intelligent, energy-efficient, and scalable architectures that can meet the growing demands of modern healthcare technologies.

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