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Power Quality Improvement in Grid Connected Photovoltaic System with Three Level Neutral Point Clamped Inverter

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Abstract

The efficient interleaved boost converter (IBC) combined with the 3-level neutral point clamped (NPC) inverter for grid-connected photovoltaic systems (GCPVS) maximizes solar energy efficiency are presented. Enhancing power quality at the Point of Common Coupling (PCC) while utilizing the rated capacity of the inverter into consideration is the main goal of the proposed approach. The grid connected photovoltaic system includes an efficient three-level NPC inverter and interleaved boost converter to decrease DC link voltage oscillation. In addition to preventing overheating, the inverter current controls reactive power adjustment, active power injection, and current harmonic filtering. Using MATLAB, the proposed topology is implemented, and the results are contrasted with those of other existing techniques. The proposed method attains a THD of 2.5%. The proposed technique displays the efficiency is 95%. When compared to existing strategies, the proposed technique displays lower THD and high efficiency.

Introduction

Today, PV systems are most likely and a well-known way to use solar energy. A type of active solar technology is photovoltaic. Voltage and electric current are induced in the substance when the solar cell is exposed to sunlight. Photons are invisible particles released by sunlight. The photovoltaic effect, often known as photovoltaic and it is the name given to this method for producing electricity directly from solar radiation. The photovoltaic (PV) system is made of PV panels containing numerous PV cells called modules, power inverter, battery controller and the utility load. Today, PV systems are most likely and a well-known way to use solar energy. A type of active solar technology is photovoltaic. Voltage and electric current are induced in the substance when the solar cell is exposed to sunlight. Photons are invisible particles released by sunlight.

The photovoltaic effect, often known as photovoltaic and it is the name given to this method for producing electricity directly from solar radiation. The photovoltaic (PV) system is made of PV panels containing numerous PV cells called modules, power inverter, battery controller and the utility load. The major goal of the proposed strategy is to decrease DC voltage fluctuation and enhance PQ. On the grid side, an interleaved inverter is used. It has 4 legs, each of which has a power electronic switch and a diode. The interleaved inverter arrangement prevents the shoot through phenomenon. When interleaved inverters are used, system performance is improved. Power harvesting and harmonic reductions are the two components of the proposed approach functioning. The NPC strategy is used to minimize harmonic distortion and avoid DC link voltage fluctuation with NPC, while the LSE method is used to harvest the most

power possible from PV. This NPC offers a lower switching frequency; as a result, switching losses are less. By that time, the IBC-NPC methodology has been implemented in MATLAB site, and its performance has been evaluated in comparison to existing methods. The simulation result shows that the IBC-NPC strategy offers 2.12% THD and improves PQ. IBC consists of two conventional boost converters connected in parallel and operates in interleaved fashion. Inductor L1, Switch S1, and Diode D1, forms the first converter while L2, S2 and D2 constitute the second converter. The two phase IBC share the same filter capacitor CO at the output.

It is assumed that the parameters of the two converters are identical. In case of the two phases, each phase control signal is shifted from each other by 180°. Switching sequences of each phase may overlap depending upon the duty ratio D.

The contribution of this paper is as follows:

- To improve the PQ produced by the photovoltaic system
- To improve the effectiveness of photovoltaic system
- The 3-level NPC inverter enhances the power quality delivered to the grid by controlling reactive power adjustment, active power injection, which prevents overheating and ensures stable grid connection.
- The major aim of the proposed method is employed to minimize the THD and enhances the efficiency of the system.
- The IBC minimizes input current ripple and reduces switching losses, leading to improved efficiency in converting solar energy into electrical power.
- The system's inverter controls are designed to manage both reactive and active power effectively, contributing to improved grid stability and efficient energy utilization.

This paper's remaining sections are organized as follows. The work's component modeling and methodology are provided in Section II. Experiments and simulations are given in Section III and IV concludes with findings.

Proposed Methodology

Proposed block diagram of power quality improvement in PV System is represented in figure. 1. The proposed method has grid, PV module, ripple filter, boost converter, MPPT and non-linear load. The proposed framework is structured on multi-functional operations including maximizing power extraction, minimizing harmonics, and enhancing PQ. The interleaved inverter has 4 legs, each of which has a power electronic switch and diode. The design of the inverter lessens the shoot-through effect. To maintain dc voltage, a capacitor is connected to the inverter's dc side. The point of common coupling (PCC) is used to fed the grid with the generated PV power. The interface inductor serves as a sort of intermediary between the grid and the photovoltaic.

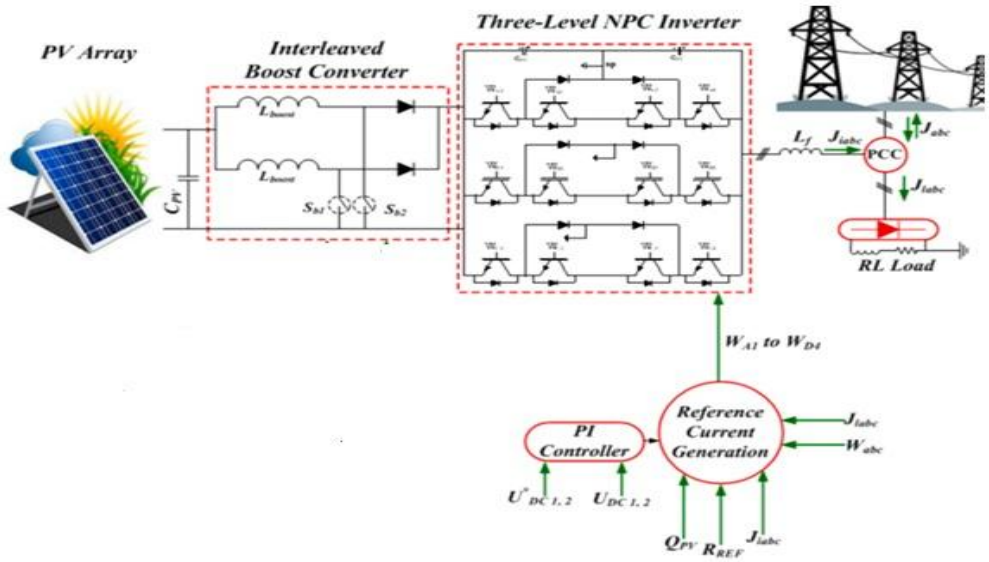


Figure. 1. Proposed block diagram of power quality improvement in PV System

In grid-tied PV systems, the NPC technique is proposed to enhance PQ. The IBC strategy eliminates harmonics while the NPC method locates the farthest distant PV power source. The ripple filter reduces the higher order harmonics. The NPC methods primary goal is to lower harmonics and improve PQ.

A. Solar PV System

PV arrays are made up of many PV modules that are associated in series to improve voltage and in parallel to improve current so that they can satisfy the demands of the load [33]. The surface temperature and sun irradiance are the two key factors that affect these goals.

The voltage of the PV array is determined by,

$$V = \left(\frac{N_s \in ZT_a}{Q}\right) ln\left(\frac{N_p G I_{ph} - I + N_p I_0}{N_p I_0}\right) - \left(\frac{N_s I R_s}{N_p}\right) \quad (1)$$

where the total number of series and parallel connected cells are denoted by N_S *and* N_p, Series resistance is represented by R_s , I_{ph} is the PV Module photocurrent, Leakage current is denoted by Io, and G stands for irradiance. Electron charge is denoted by Q, Z is the Boltzmann coefficient, Surface temperature is denoted by T_a, e for completion factor. Trackers can monitor the PV module's maximum power point.

NPC have been employed to follow the highest power in order to attain this goal. The incremental conductance (INC) methodology is one of them that is frequently utilised. This technique is used to control the PV system's IBC converter's duty cycle. The transfer functions of the PV system are expressed as

$$G_1 = \left(\frac{s^2}{s^2+\omega^2}\right)\left(\frac{V(s^2+\omega^2)(s^2+2\omega^2}{ks^2(s^2+4\omega^2)}\right)\left(\frac{1-e^{-sT_s}}{sT_s}\right) \quad (2)$$

$$G_2 = \left(\frac{\frac{M_1}{LC}}{s^2+\frac{1}{RC}s+\frac{1}{LC}}\right)\left(\frac{1-e^{-\frac{sT_s}{2}}}{1+e^{-\frac{sT_s}{2}}}\right)\left(\frac{M_2}{1+sT_s}\right) \quad (3)$$

where w stands for the electric grid angular frequency, R, C and L stand for the converter's output characteristics, M_1 is the gain voltage of chopper network, M_2 is the gain voltage of the inverter, and Ts is the sampling interval. An inverted diode and a power supply are typically connected in parallel to form a solar cell. It represents series and parallel connections, respectively, using series and parallel resistors. Series resistance results from a disturbance in the path of electron movement from the n-p junction, whereas leakage currents result in parallel resistance [13]. The solar PV system's network diagram is represented in Figure .2.

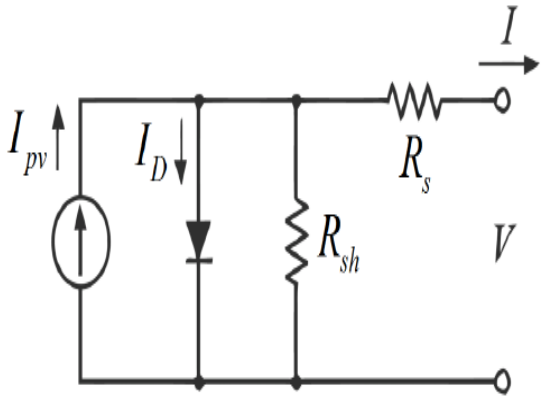


Figure 2: Circuit diagram of PV

The following equation represents the PV current at the output end:

$$I = I_{scc} - I_d \quad (4)$$

$$I_d = I_O\left(e^{\frac{qV_d}{KT}} - 1\right) \quad (5)$$

where V_d = Diode Voltage, k = Boltzmann constant ($1.38 \times 10^{19}\ J/K$), Io= reciprocal of the diode current saturation, I_{scc} = Short circuit current of a PV panel, I_d = Diode Current, q= Electron charge.

By solving Equations (4) and (5)

$$I = I_{scc} - I_O\left(e^{\frac{qV_d}{KT}} - 1\right) \quad (6)$$

By proper estimates,

$$I = I_{scc} - I_O\left(e^{q\left(\frac{V+IR_s}{nKT}\right)} - 1\right) \quad (7)$$

where I, V, and n stand for the diode ideal factor, Voltage of PV cell, and PV cell current, respectively.

B. Interleaved Boost Converter

The two phase interleaved boost converter is as shown in Figure.3. It consists of two conventional boost converters connected in parallel and operates in interleaved fashion. Inductor L1, Switch S1, and Diode D1, forms the first converter while L2, S2 and D2 constitute the second converter. The two phase IBC share the same filter capacitor CO at the output. It is assumed that the parameters of the two converters are identical. The gating signals and the inductor current waveforms of the converter are shown in Figure.3.4. In case of the two phases, each phase control signal is shifted from each other by 180°. Switching sequences of each phase may overlap depending upon the duty ratio D.

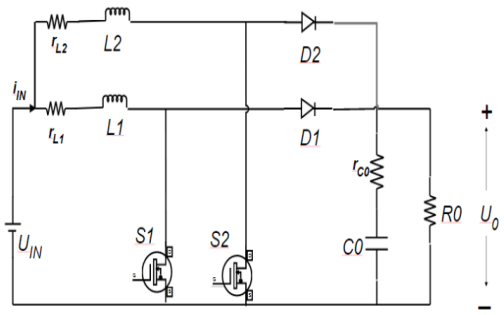


Figure 3. Interleaved Boost Converter

Switches are ON simultaneously. R2 will be discussed in detail in the following sections for continuous conduction mode (CCM).

Working principle

In region R2 and considering CCM operation, the proposed converter has four topological stages per switching period that can be described as follows. Before the first stage, S2 is already conducting.

Stage 1 (0<t<t1)

Stage 1 starts when switch S1 and S2 are turned on and the diodes D1and D2 are reverse biased. Inductor L1 and L2 are magnetized with energy from power source UIN and current iL1 and iL2 increases linearly as shown in the figure 2. The load receives energy from the output capacitor CO. This topological stage is shown in figure 4.

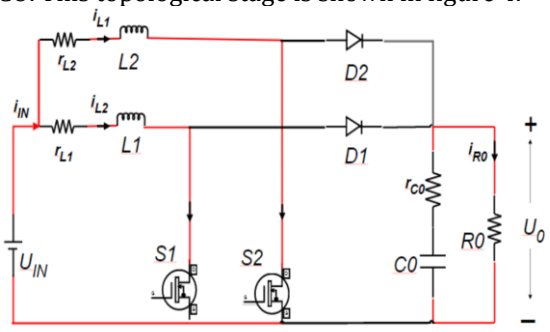


Figure 4. Equivalent circuits of first third and fifth stages

Stage 2 (t1<t<t2)

This stage starts when switch S2 is turned off and hence diode D2 is reverse biased. Inductor L2 is demagnetized and current iL2 decreases linearly. The load receives energy from the source and the inductor through diode D2. This topological stage is shown in figure 5.

Stage 3 (t2<t<t3)

The third topological stage is same as the first stage.

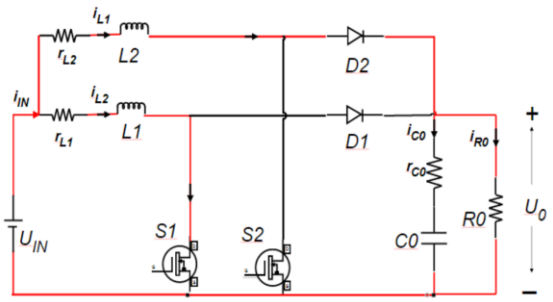


Figure 5: Equivalent circuit of Second stage

Stage 4 (t3<t<t4)

This stage starts when switch S1 is turned off and hence diode D1 is reverse biased. Inductor L1 is demagnetized and current iL1 decreases linearly. The load receives energy from the source and the inductor through diode D1. After the fourth stage, the switching period is complete and another period starts with the first stage.

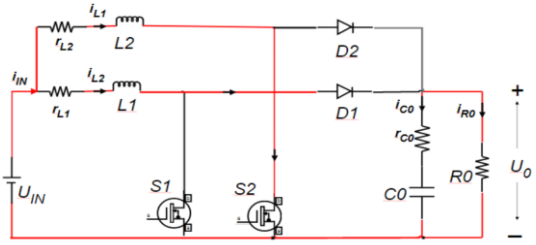


Figure 6. Equivalent circuit of fourth stage

Table 1: Design Specification

Input voltage	10V
Output voltage	20
Output power	25Watts
Switching frequency	31 kHz
Input current ripple	5%
Output voltage ripple	2%

C. Three Level Neutral Clamped Inverter

One appropriate topology for usage in high power systems is the 3- level NPC inverter. The 3-level NPC inverter's circuit structure is the cause. Two switches are present in each phase of 2-level converters, which were often used [16]. As a result, one switch must withstand +Vdc 2/ or - Vdc 2/ of voltage stress. When a switch flips from a positive to a negative state, it may also be momentarily subjected to voltage stress of Vdc, which might reduce the switch's lifespan. All phases of the 3- phase, 3-level NPC inverter, however, consist of 2 diodes and 4 switches. Thus, two switches can disperse the voltage stress of +Vdc 2/ or - Vdc 2/ , in contrast to two-level converters. Figure 7 shows the Power Circuit of 3-L NPC Inverter.

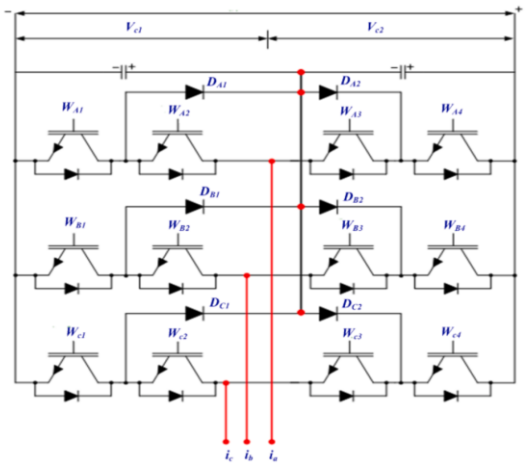


Figure 7. Three level NPC Inverter

A 3-phase, 3-level NPC inverter features two diodes (DX1 and DX2) - and four switches (WX1, WX2, WX3 and WX4) in each phase. The midpoints of diodes DX1 and DX12 are are linked to the NP, while the midpoints of switches WX2 and WX3 of each phase are linked to the load. The direct current - link's upper and lower capacitor voltages must be changed in order to maintain equilibrium. According to Table 1, the 3 - level inverter may create pole voltages of + Vdc 2/ , 0 and - Vdc 2/ , respectively, and 3 voltage levels, P, O, and N, based on on the switching condition.

Results And Discussion

An efficient IBC with a 3-level NPC inverter for a grid connected photovoltaic system maximizes energy efficiency. Simulation is a powerful way to reduce development time and ensure the proper fulfilment of critical steps. During the development process of the shunt active filter, simulations were performed, which allowed the study of its behaviour under different operation conditions, and permitted the tuning of some controller parameters together with the optimisation of the active filter components values. There are not many simulation tools that allow working with electrical systems, power electronics and control systems, in the same integrated environment. Matlab/Simulink and the Power System Blockset were used as simulation tools in this paper. In this, the performance of the proposed approach is evaluated

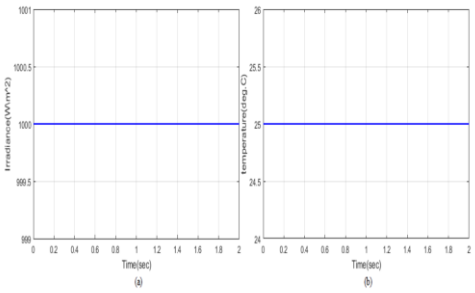
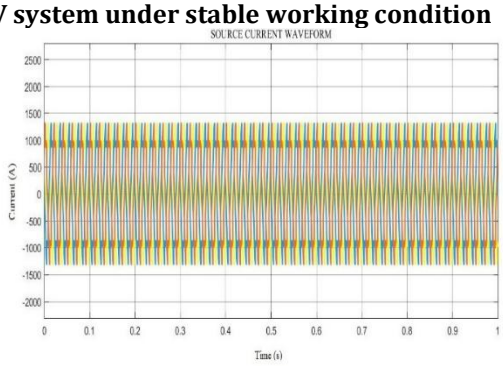


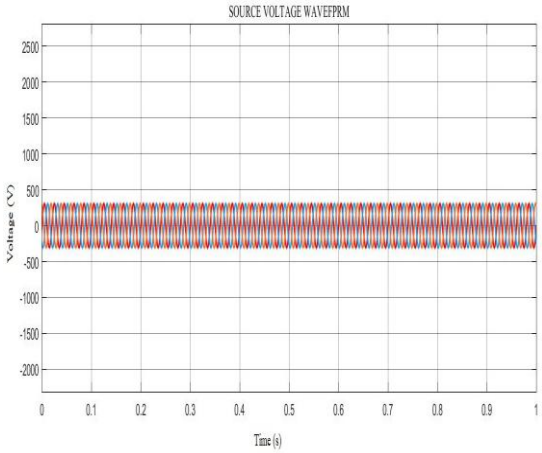
Figure 8. Investigation of Reference a) Irradiance and b) Temperature

Figure 8 depicts Investigation of Reference (a) irradiance, and (b) Temperature. Figure 8 (a) depicts reference irradiance. From 0 to 2 seconds, the reference irradiance is fixed at 1000 W/m2. Figure 8 (b) depicts reference temperature. From 0 to 2 seconds, the reference temperature is fixed at 25 W/m2.

PV system under stable working condition

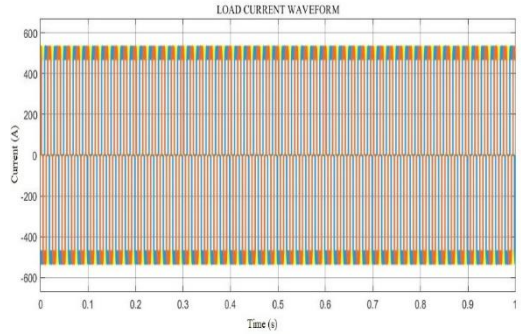


(a)

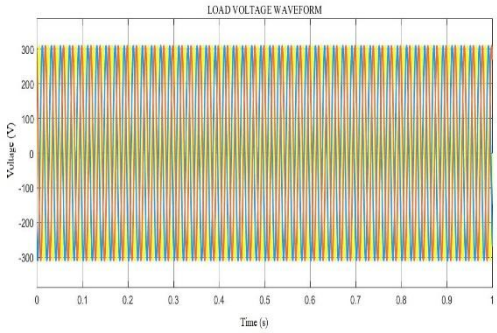


(b)

Figure 9. Source voltage and current waveform under stable condition



(a)



(b)

Figure 10. Load voltage and current waveform under stable condition

Figure 9 represents the Source voltage and current waveform under stable condition, where the value of current is 1200A and the value of voltage is 400V. Figure 10 represents the Load voltage and current waveform under stable condition, where the value of current is 500 A and the value of voltage is 300V.

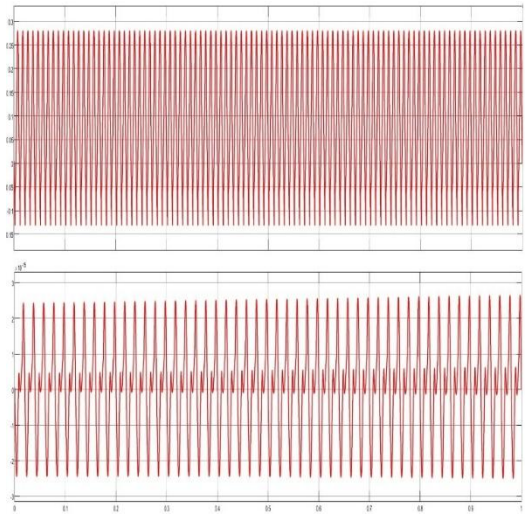
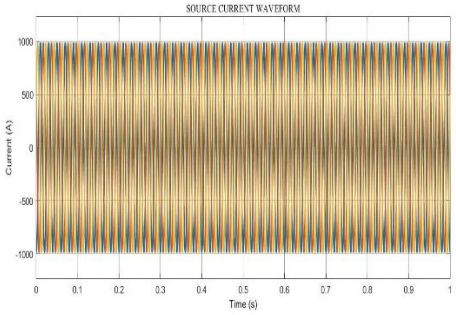


Figure 11. Active and Reactive power waveform under stable condition

Figure 11 shows the Active power and Reactive power waveform, where the value of active power is 0.25W and the value of reactive power is -2.5 to 2.5W.

PV System under varying condition:



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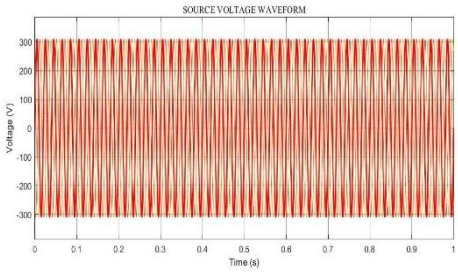
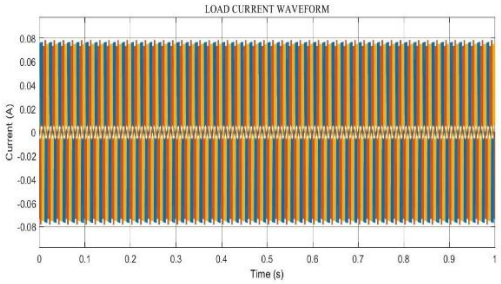


(b)

Figure 12. Source voltage and current waveform under varying condition



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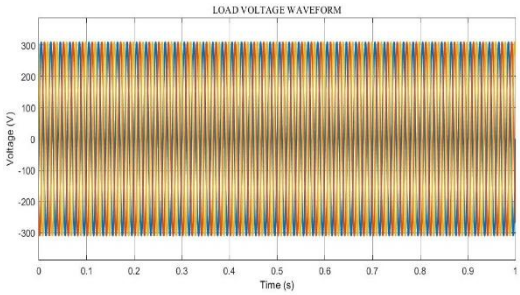

(b)

Figure 13. Load voltage and current waveform under varying condition

Figure 12 represents the Source voltage and current waveform, where the value of current is 1000A and the value of voltage is 300V. Figure 13 represents the Load voltage and current waveform, where the value of current is 0.08 A and the value of voltage is 300V.

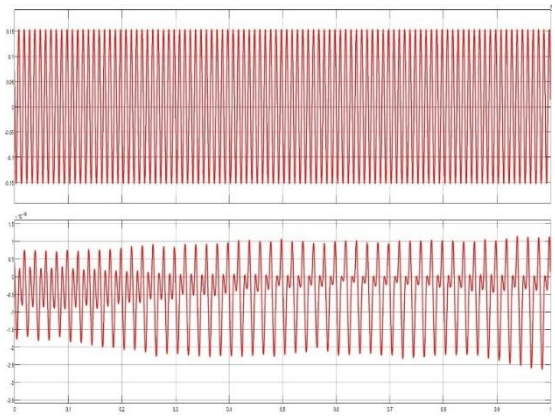

Figure 14. Active and Reactive Power waveform under varying condition

The active power is that amount of the total electric power in an AC electric circuit which actually consumed or utilized. It is also called as true power or real power. Figure 4.8 shows the Active power and Reactive power waveform, where the value of active power is 0.15W and the value of reactive power is -2.5 to 1W.

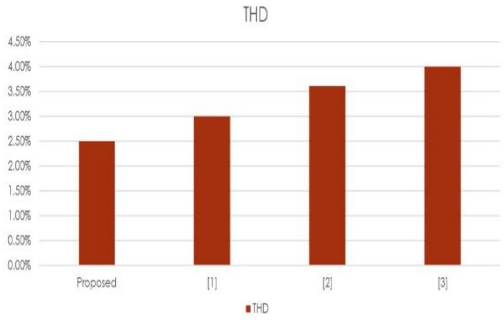

Figure. 15. THD Wavefrom

Figure. 16. Efficiency waveform

A comparison of performance is presented in Figure 15 and 16. In comparison to the previous works, the proposed converter outperforms all with the highest efficiency of 98%. In previous converters such as ACFF of 92.86%, single-phase interleaved buck-boost converterof 93%, and Boost PFC converter of 95.92%.

Conclusion

In this section, an effective interleaved boost converter is combined with a 3-level NPC inverter for GCPVS. The primary aim of the presented technique is to maximize the energy efficiency and minimize the THD. Additionally, a three-level NPC inverter and an efficient IBC are provided to reduce DC link voltage oscillation in the GCPVS. In addition to controlling the GCPVS's reactive power adjustment, active power injection, and current harmonic filtering capabilities. By employing the IBC-NPC technique, the system effectively regulates output voltage, ensuring that the inverter output voltage. The IBC-NPC enhances the system's ability to monitor and diagnose faults. Implementing the proposed topology with the MATLAB platform and the outcomes are contrasted with those of alternative techniques. The proposed approach achieves a THD of 2.5 %. The proposed method efficiency is 95 %. The proposed approach gains less THD and higher efficiency in comparison to current methods.

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